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HIGH CURRENT ESD DAMAGE TO MOS I/O STRUCTURES CAUSED BY CHARGED VIDEO MONITOR SURFACES AND CASINGS

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ABSTRACT

A case study of a high current ESD phenomenon associated with handling MOS ICs in the vicinity of charged computer CRT terminals is presented. Component I/O metal damage occurred on an automotive module assembly line, and required special circuit modeling to explain and reproduce the damage. The phenomenon, the model, and the corrective design solution are discussed.

I. INTRODUCTION

This paper will present a case study of a peculiar and puzzling EOS/ESD problem that was encountered on a automotive custom SRAM. We will begin by describing the background and environment of the EOS/ESD event on the factory floor. We will present three possible scenarios for occurrence of the EOS/ESD event, and relate these to simulation tests and failure analysis. At the end we will discuss our design solution to the problem and the actual effect that it had. This case study proved to be a true "slice of life" in EOS/ESD problem solving.

II. BACKGROUND

MOS IC components (p-well CMOS custom SRAM) returned from a customer assembly site indicated ESD damage, as shown by output metal lines being blown, stressed, and cracked (Figure 1). It was puzzling that the component had previously passed all Charged Device, Human Body Model (HBM or Mil Spec), and Machine Model (MM) testing for part qualification. A recheck of these ESD tests again showed no failure until well above the specification voltage limits. These events drove the investigation to the following theory and corrective design solution.

III. ESD PHENOMENON AND MODEL

Since the part passed all regular ESD requirements, the investigation turned to the customer's facilities and their ESD control policies and practices. At the customer's assembly site, we checked numerous possibilities, from spurious tester driver overshoots to human and assembly line handling practices.

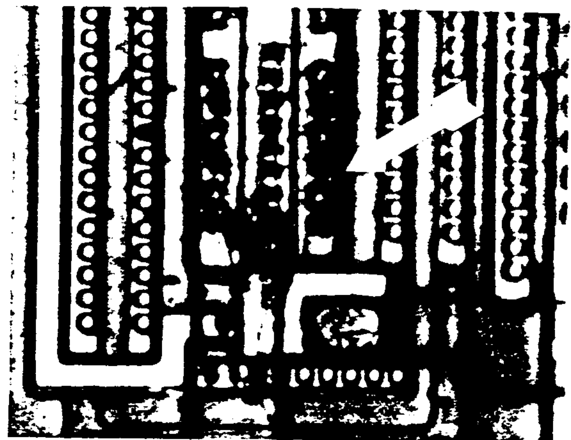

Figure 1: Photograph of blown output metal lines from customer's return part.

Soon the possibilites narrowed to the handling and storing of modules (modules are board-level units containing the custom SRAM) on the assembly line. A visiting Intel engineer observed that excess modules were removed from the assembly line, stacked on metal trays, and stored where space permitted until later. One noteworthy storage location for the trays was on the tops of computer terminals near the assembly line. This gave rise to the notion that a large amount of positive charge (due to the positive accelerating voltage of a CRT) was collected by the tray and modules, somehow causing the SRAM damage when it was dissipated.

Before we discuss the electrical modeling of the failure, we will describe the assembly station in further detail. The modules are passing by the station on a conveyor belt, coming from a machine that sprays a fully assembled module PC board with a final hermetic plastic sealer. Because there are

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some difficult spots on the module PC board that do not get a uniform coating of the spray, a worker at this station hand sprays and touches up the modules that did not get a complete uniform coating of the hermetic plastic sealer. The worker is wearing a plastic apron and rubber gloves for protection from the chemical spray. When the worker runs out of the hermetic sealer in the bottle, he ("he" will be used to denote "he or she") must stop to refill the bottle. In the meantime modules are continually coming by the station on the conveyor belt. To prevent any modules from passing by without inspection, modules are taken off the conveyor belt and placed on metal trays for temporary storage while a service person refills the worker's bottle with the hermetic sealer. These modules are reworked when time is available. Some trays with modules were routinely placed on assembly and inventory control computer video terminal tops near the spray station, and of course those modules are believed to have been threatened by ESD. Table tops in the vicinity of the station, including table tops for the video terminals, were connected solidly to earth ground.

We arrived at three possible scenarios for the ESD event, each relating to ways in which the charge on the tray and module can be dissipated through the component, causing destruction. Beginning with the most likely, they are

1) Someone lays an uncharged module on an empty charged tray already sitting on top of a terminal, triggering the event.

2) Someone touches a charged module on a storage tray sitting on top of a terminal, triggering the event.

3) An uncharged module (or modules) sits on top of a terminal, and enough potential builds up that the tray arcs to it.

Although all three scenarios are possible, we think that scenario number one, where a worker places an uncharged module onto a charged tray, is the most likely in light of the assembly station conditions. First we will briefly discuss the last two scenarios.

Scenarios number 2 and 3 are less likely to occur in this environment. For scenario 2 to cause a sudden discharge, the worker would almost have to remove his insulating rubber gloves when taking the modules off the tray to be reworked, not a common occurrence on this assembly line. For scenario 3, where an arc sparks from the tray to the backside of a module's PC board, there would have to be some reason why the arc occurred after the human hand was removed, or else we would have scenario 1. As we continue the discussion, it will become clear that the electrical effect of all three scenarios is very similar.

Based on known events at the station, our primary scenario involves modules being placed on a charged tray sitting on the computer video monitor top. When the worker's bottle becomes empty, he takes off his rubber gloves to unscrew the reservoir bottle from the hand sprayer for the service person to refill. While the service person is refilling the reservoir bottle, he removes the modules coming down the conveyor belt without wearing his rubber gloves. Then he slides the module onto a metal tray such that the backside of the PC board approaches or touches the charged tray sitting on the computer terminal top. This is where the circuit is closed. The excessive tray charge collected on the tray is discharged through the component to the worker's hand.

Typical plastic video monitor surfaces and casings can be charged up to a high voltage basically because of the high accelerating voltage for the electron beam in a CRT. Charge is particularly evident on the CRT screen. Sample electrostatic field meter readings show static charge ranges from 1,000 to 35,000 volts depending on type. Normally the high resistance plastic prevents the static charge from being mobile. With the large metal tray placed on top of the terminal, the tray shorts out the high resistance (Figure 2) and allows the charge to be collected at a single point. The quantity of charge stored is large and is capable of supplying enough energy to do metal damage. In a sample re-creation with a small 45 cm X 45 cm sheet metal tray charged to 3.0 K volts, 330 nC was discharged from the tray (i.e., Ctray was found to be 110 pf). If this charge is given the chance to discharge to ground or have an opportunity to equalize potentials with other PCB trace capacitances or people, it will cause metal damage (Figure 1).

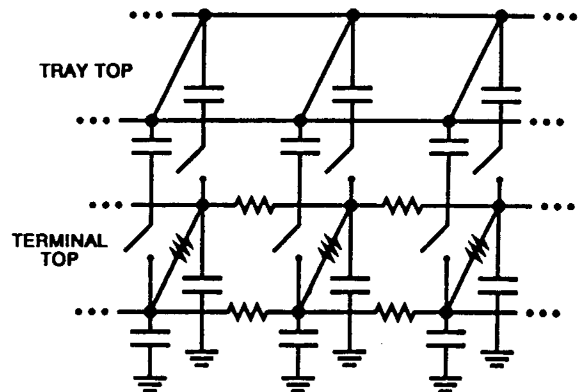

Figure 2: Tray/Terminal top charge coupling schematic.

Our model was derived by characterization of the ESD event. Figure 3 is our basic model (scenario #1). Figure 4 illustrates our model applied to the 3 scenarios. The values of the components were measured or derived directly from the module itself where the custom SRAM is used. Most of the capacitor and resistor component values were measured with an LCR meter and other capacitance values were calculated from storage scope traces of a capacitive discharge through a known resistor. Following are the circuit elements used in Figure 3:

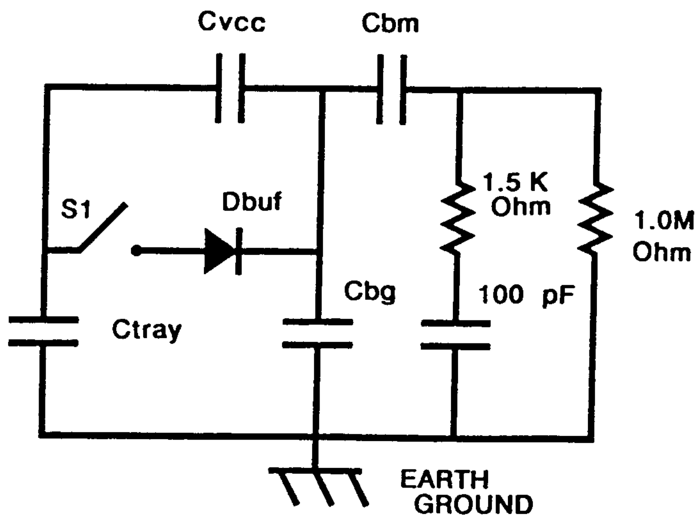

Figure 3: Basic circuit model of ESD phenomenon (Scenario #1)

Cbm - The capacitance between the module casing and VCC board trace

Cvcc - The capacitance between VCC board trace and the tray

Cbg - The capacitance between the VCC board trace and ground

Cmg - The capacitance between the module casing and ground

Dbuf - The output buffer P-N junction diode (p-channel pullup device between pad and Vcc; this has low resistance because the N-substrate is tied to Vcc in P-Well CMOS)

Ctray - The capacitance between the tray and ground when it is on top of a terminal

Rst - The 1 Megohm resistance of the worker's ground strap. This is appropriate because the worker is likely to be grounded even if not wearing a strap.

HBM - The 1.5 K resistor and the 100 pF capacitor is the Human Body Model (HBM) of the worker.

S1 - Switch 1, where an arc from the tray sparks across to the back side pins of the PC board traces

S2 - Switch 2, where the worker touches the module or the back side PC board traces

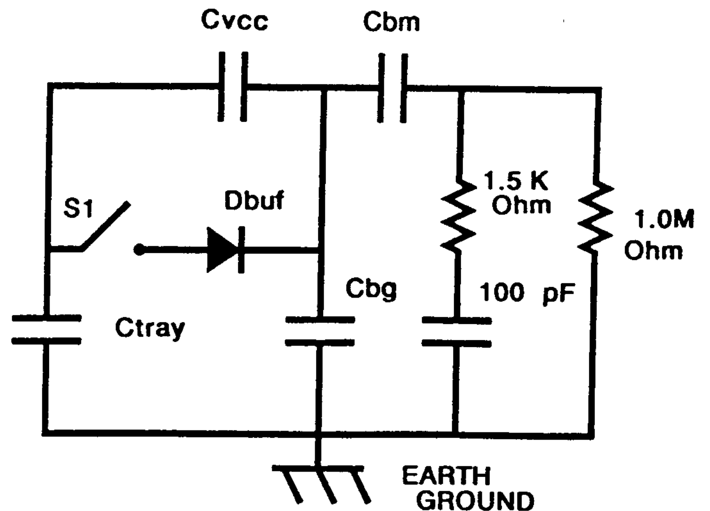

Figure 4a: Circuit model of Scenario #1. Someone lays an uncharged module on an empty charged tray sitting on top of a terminal.

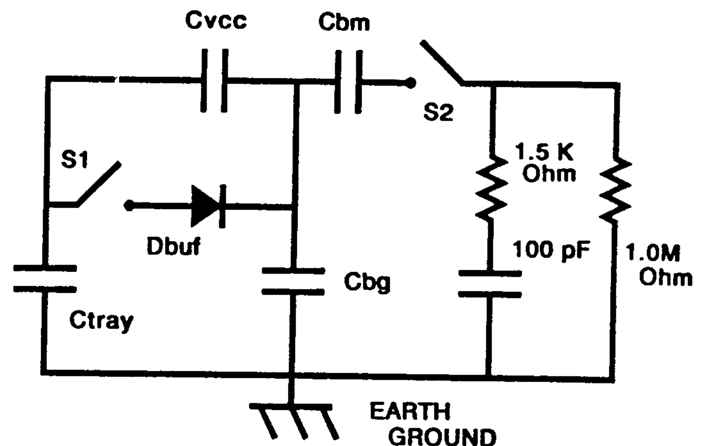

Figure 4b: Circuit model of Scenario #2. Someone touches a charged module on a storage tray sitting on top of a terminal.

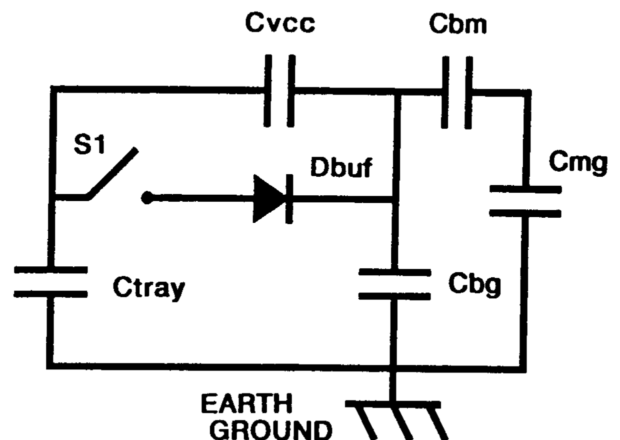

Figure 4c: Circuit model of Scenario #3. An uncharged module sits on top of a terminal and the tray arcs to it.

Our primary scenario (#1) happens in the following way. An empty tray, sitting on top of computer display terminal, collects charge and reaches voltage Vtray, which can be thousands of volts. When the worker touches the module and slides it onto the tray, the module is angled so that the backside of the PC traces touches or an arc occurs between the PC traces and the tray (closing switch 1) causing the tray top to discharge Ctray and Cvcc through the component to the worker. (Note that Cbm is quite large and behaves almost as a short.) In this model of scenario #1, a machine model-like event best describes the discharge of Cvcc. When the arc forms to charge Vcc, charge passes though the diode Dbuf to neutralize the voltage across Cvcc. Cvcc is dependent on the module's distance from the tray top, but in its final position Cvcc is the highest (as readily measured and shown in the figures), and any charge on Cvcc in that position will have to be dissipated. Cvcc at 78 pf is at about 40% of the usual machine model value of 200 pf (Figure 5), so the machine model (MM) failure voltages would have to be scaled up to be equivalent to this case. If the failure relates to total energy in the capacitor (as we will argue is likely), the voltage scale factor between the MM and the module arc event would be about 1.6 (square root of the capacitance ratio).

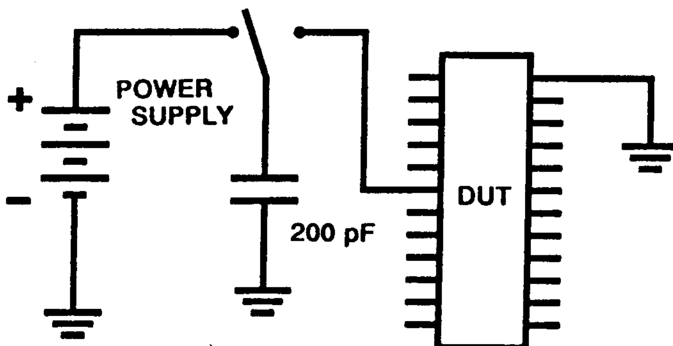

Figure 5: Machine Model, 200 pF capacitor and zero resistance to DUT

We also see an HBM event after Cvcc discharges. Cbm acts as a virtual short as Ctray charges up the person holding the module. This is an HBM event as far as Dbuf is concerned, although the equivalent voltage is about half the voltage on the tray, since Ctray is about equal to the HBM capacitance.

Finally, notice that Ctray can be recharged by the terminal and arc to Vcc again, until Vcc is charged to the original voltage on Ctray. This means that multiple discharges can occur quickly, although none should be more severe than the first.

This event caused an EOS-like failure characteristic with ruptured I/O metal lines, yet it is truly an ESD event. We now turn to a discussion of our efforts to re-create the ESD damage.

IV. ESD PHENOMENON SIMULATION/CHARACTERIZATION

In the early stages of this effort, the complete circuit model of the event as discussed above was not yet clear, and we had rejected all of the traditional ESD test models because the part passed those tests. At this point, under time pressure to design and evaluate a layout solution for the problem, we developed a bench top simulation model to re-create the damage. We used a 22 uF capacitor charged up to 5.0 volts (Figure 6).

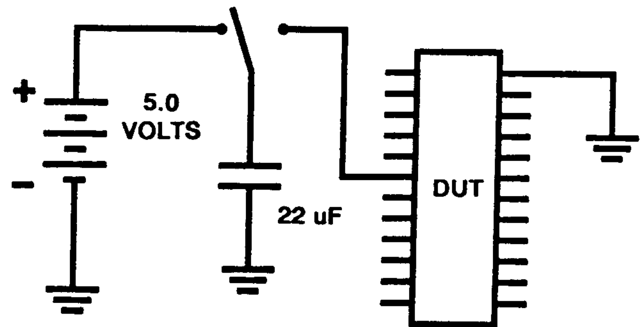

Figure 6: Bench top re-creation, 22 uF capacitor charged to 5.0 Volts and discharged into DUT.

This test was meant to approximately reproduce the ESD damage, and to later verify the proposed design fix to the problem. Only later did it become clear that a machine model-like zap was occurring to the device, and at an equivalent voltage level far above the usual 200V test voltage.

We arrived at the values for the bench top simulation after characterizing the output driver P/N junction on the curve tracer. A constant 600 mA of current caused the I/O buffer P/N junction (with an "on" resistance of 4 ohms) to fail. 5 volts and 22 uF was a somewhat arbitrary choice of RC discharge conditions that delivered a measured quantity of charge with similar voltages and currents, and did cause destruction resembling that of the units returned from the assembly line. The RC of this circuit with the "on" diode resistance was 88.0 uS, the average instantaneous current, Q/RC, was 1.25 Amps, and the available stored energy, was 275 uJ.

When the circuit modeling effort renewed our interest in the machine model, we later returned to machine model testing, in search of a better simulation of the ESD damage in the returned units. Earlier MM testing, as we have said, did not produce failure until about 800 V, well above the 200 V specification. Also, there was minimal visible damage at that threshold of failure, in contrast to the units returned from the field (Figure 1). But since the energy required to destroy the metal with the 22 uF capacitor was so large (275 uJ, above), there was good reason to look at how parts failed on the machine model at higher voltages.

From about +900-1500 V on the machine model (negative zaps do not cause failure until much higher voltages, and do not relate to our damage model), there was little visible damage and failure was due to leakage current above the specification limit of 1 uA. Around 1500 V and above we began to see the same failure characteristics in the same failure location as in the returned units from the factory floor (Figure 7; note similarity to

Figure 1). As we approached 3000 volts, the leadway metal line from the bond pad ruptured and evaporated. All the MM capacitor energies in the higher voltage tests were in the same range of energies as the 22 uF model. For example, the MM tests at 900V and 1500V, respectively, produced 81 uJ and 225 uJ, which is just below but approaching the 275 uJ destruction energy of the 22 uF model. This also supports the notion that MM capacitor energy, not voltage, determines the failure, and means that MM voltages should be multiplied by 1.6 (square root of capacitance ratio, see Section III) to be equivalent to our "real world" model. We thus conclude that high voltage machine model events were destroying the parts. This is quite acceptable, as there is no requirement for such physical phenomena as metal tray discharge to occur at the threshold of destruction of our component!

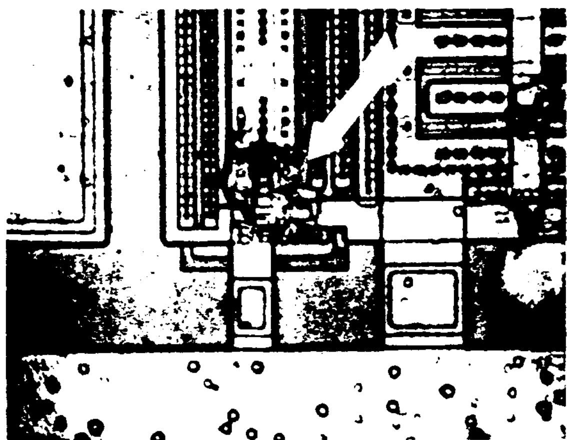

Figure 7: Photograph of blown output metal lines from high voltage Machine Model testing. Note similarity to Figure 1, return part from customer.

One more comment about the Human Body Model is in order. In Section III we described how an HBM pulse accompanies the MM pulse when the tray discharges through the I/O pin. The MM pulse is what fails the device, however, because while the MM test fails at 800-900 V, the HBM test does not fail until 6 kV or more. From our previous arguments, a charging voltage Vtray on the metal tray will produce an equivalent Vtray/1.6 MM stress, and an equivalent Vtray/2 HBM stress. Thus the Vtray for HBM failure (12kV) is about 8.3X higher than it is for MM failure (1.44kV), indicating that the HBM pulse is no threat.

Note that while the machine model is relevant to this ESD problem, the part easily passed the 200V MM test standard and was not considered susceptible to ESD until the factory problem occurred. The factory problem was not avoided by any kind of reasonable compliance to MM or other familiar ESD tests, because the factory conditions induced MM-like ESD stresses to thousands of volts, far in excess of reasonable MM standards. This case thus cannot be seen as any kind of endorsement for the machine model as a standard ESD test. In this case, it turned out to be far more important to remove the source of ESD stress by improving the handling practices in the factory. However, these problems tend to be solved by some kind of multi-pronged attack, even if it appears that one activity will be crucial. We also executed a design change aimed at improving the performance of the device when subjected to this kind of ESD stress.

V. CORRECTIVE DESIGN SOLUTION

To limit the high current pulses through the I/O buffer P-N diode, a current limiting poly resistor was placed in series with the p-channel output drain and the output pad (Figure 8). The series poly resistor not only limited the current from the high current pulses, but also tended to divert any high voltage arcs away from these sensitive I/O pins, with their now higher resistance path to Vcc. The value of the resistor selected (50 ohms) was selected with the breakdown failure current, Voh/Vol specifications, and NPN snapback voltage of the ESD protection device in mind. Other poly resistors were made available addition to the primary choice resistor through mask programming, but were not needed. Other design changes included widening the I/O metal line, redistributing contact resistance on the p-channel output driver, and increasing metal spacing in key locations.

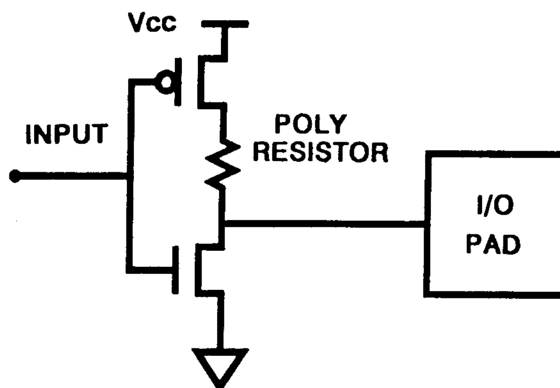

Figure 8: Schematic of design fix to I/O buffer with polysilicon resistor in series with P-Channel transistor.

VI. RESULTS

The parts with improved I/O circuitry showed substantial improvement in our 22 uF capacitor discharge test but only slight improvements for the regular ESD tests, including the machine model. The poly series resistor protected the p-channel half of the output buffer quite well, although damage was shifted to the n-channel output FET. Even at the higher machine model voltages (up to at least 2500 volts), the ESD leakage and damage occurred only on the n-channel pulldown FET device.

This design fix was considered successful some time before we completed the circuit modeling effort, at which time we recognized the special importance of the machine model. So why, we asked, was the design fix successful even though it caused little

improvement in MM performance? The best answer is that the 50 ohm poly resistor made the I/O pin less able to act as a "lightning rod" for equalizing metal tray and module Vcc potentials, since it now had a high resistance path that served to divert or extinguish an arc. The arc that does equalize these potentials was now most likely to form somewhere else, as between the tray and the actual Vcc trace, causing a harmless transfer of charge. Thus the 50 ohm resistor fix can be seen as being serendipitously successful (recall our earlier promise of a "slice of life"). With this fix and some improved assembly and handling practices at the assembly site, thousands of units have been in production without any additional returns for ESD failure.

VII. SUMMARY

A new high voltage and high current ESD event was demonstrated, one that caused melting of metal in a low-resistance integrated circuit path. It was also demonstrated that charge can be collected from non-conducting surfaces such as computer tops with a large metal collector, which can act as a high current source to cause damage. Circuit models for the ESD event were fully developed, and the ESD damage was best reproduced by doing a machine model ESD test at a very high voltage.

The corrective design solution for the new ESD event was successful. The poly series resistor and widened metal lines on the I/O pins provided more margin to regular ESD testing, but probably gained their biggest advantage from the resistor's ability to discourage the damaging arcs from forming at the I/O pins. The result was no further ESD failing returns from the customer.

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