TRANSMISSION LINE PULSING TECHNIQUES FOR CIRCUIT MODELING OF ESD PHENOMENA

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ABSTRACT

A charged transmission line can be used to apply high current pulses to integrated circuits, including MOSFET ESD protection devices. Arbitrary impedance of the pulse source is possible, as is suppression of unwanted reflections. I-V plots and circuit models for integrated devices can be deduced, allowing several new features of NMOS FETs to be observed. The effect of ESD pulses on isolated aluminum and polysilcon lines can be measured, and the technique can be extended to allow ESD tests on devices at the wafer level.

I. INTRODUCTION

When an electrostatic discharge (ESD) failure is observed in an integrated circuit, an analysis process aimed at identifying and solving the problem must follow. Once the location of the electrical fault is revealed, it is usually explained by supposing that the discharge current followed a particular path, causing the fault. Disagreements about which of several discharge paths are active can be put to rest by introducing an accurate circuit model, yet the tools for developing such models in the short-time, high-current regime of ESD (typically tens of nanosec and amps of current), are not generally available in the typical ESD lab. ESD simulators (Mil-Spec or human body, charged device, etc.) are of limited use because of the complexity of the waveforms they produce on the devices. We have found that the response of integrated devices to simple, square pulses (produced by charging a transmission line) on the same time and current scale as ESD events can be used to construct these needed circuit models. This new tool has allowed us to diagnose and solve ESD problems much more quickly and accurately.

In Ref. 1 these authors introduced a basic transmission line pulsing technique, one of several we will discuss here, and used it and other techniques to deduce several features of CHMOS devices that are worth repeating for the sake of discussions that follow:

a. High current, low voltage events result from ESD applied to the drain of a short-channel MOSFET.

b. An NMOS FET is likely to be ESD sensitive in reverse breakdown because of localized current flow, caused by electron trapping in the oxide.

c. The low resistance of an NMOS FET in reverse breakdown is likely to result in its taking most of the ESD current in the case of a CHMOS output, causing the n-channel device to fail first.

We will discuss several transmission line pulsing techniques in this paper, as well as their use in circuit modeling of MOSFETs and in studying ESD failure of aluminum and polysilicon lines. We will also show how the technique can be used at the wafer level, to allow meaningful ESD measurements on devices not yet diced, bonded and packaged.

II. BASIC TRANSMISSION LINE PULSING TECHNIQUES

Electrostatic discharge is a high current, fast event, usually involving a complicated voltage waveform. But the basic failure mechanisms and electrical behavior of a device influenced by ESD can be reproduced in simpler form by using brief (10-150 nanosec) constant voltage pulses produced by a charged transmission line, as introduced in Ref. 1. From the device's response to these pulses, a circuit model for the device under ESD stress can be constructed, often a considerable aid in failure analysis.

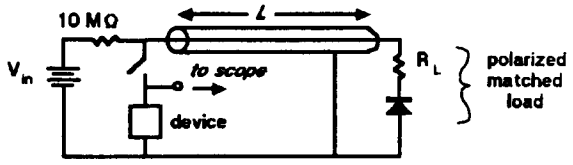

Fig. II.1. Basic transmission line pulsing setup

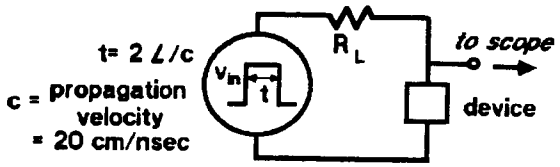

Fig. II.2. Equivalent circuit of transmission line pulser

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The transmission line pulse setup is shown in Fig. II.1. A charged 50 ohm (let us assume) coaxial cable is used to apply a short pulse (3 nanosec per foot of cable) to a device. Using a charged transmission line is conceptually similar to the more common practice of using a charged capacitor's stored energy for ESD simulation. But while the charged capacitor and a device under test produce an R-C waveform that is often disturbed by parasitic elements (notably when device resistance is low), the distributed L-C elements of a transmission line produce a pulsed voltage source with impedance equal to the line impedance ($\sqrt{L/C}$), resulting in a simple and easily intepreted waveform (Fig. II.2). Unwanted reflections from low resistance devices (less than 50 ohms) are suppressed by a polarized matched load (50 ohm resistor plus diode) at the opposite end of the line. When the negative reflected pulse from the device reaches the opposite end of the line, the diode forward biases and the 50 ohms terminates the pulse.

As shown in Fig. II.2, the transmission line of Fig. II.1 produces a voltage pulse of height V_{in}, of duration $t=2(l)/C$, in series with the transmission line impedance R_L. The pulse height is limited only by the dielectric strength of the cable and switch and is typically thousands of volts, a major advantage over most laboratory pulse sources. The instantaneous current through the device is

$$I_{device}(t) = (V_{in} - V_{device}(t))/R_L \quad (II.1)$$

Device voltage is commonly observed on a storage oscilloscope. For a purely resistive device, I_{device} and V_{device} are constant during the pulse, and the high current i-v curve is easily plotted.

A device's capacitive or inductive component will produce a time-varying current-voltage response, but usually one which allows the equivalent inductance and/or capacitance to be calculated from i-t or v-t plots. The non-reactive (resistive) component and offset voltages are determined from device behavior after the voltage has stabilized.

When devices were destroyed by the transmission line pulses, the destruction energy could be calculated by integrating the device power over time:

$$E_{des} = \int_0^t V_{device}(t) \cdot I_{device}(t) \cdot dt \quad (II.2)$$

Device destruction energy as a function of pulse width was also measured, and was more fully discussed in Ref. 1.

Fig II.3b shows device i-v curves for the constituents of a CMOS inverter (n-well technology, see Fig. II.3a), measured in the high current mode by 50-100 nanosec transmission line pulses. The concentration of current in the n-channel device for both positive and

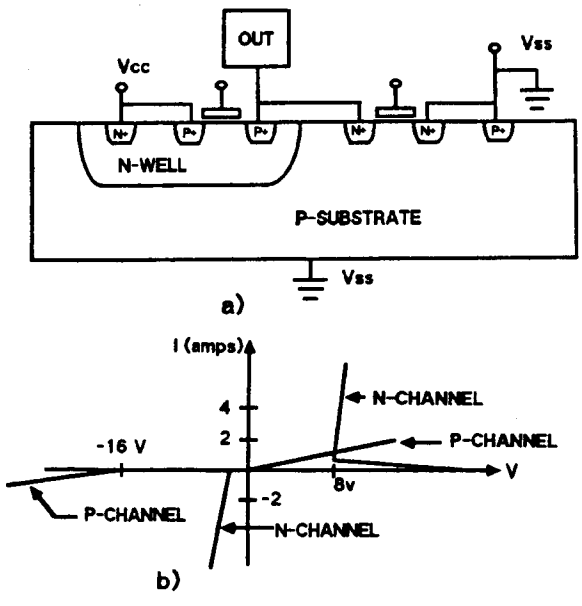

Fig. II.3. a) N-well CMOS inverter cross section. b) ESD I-V Curves for constituents of an n-well CMOS inverter.

negative pulses can easily be seen. The intrinsic resistance of a p-channel device in reverse breakdown is always higher than that of an n-channel device (traceable to mobility and carrier multiplication differences between electrons and holes), while a forward biased p-channel device in an n-well is resistive enough to provide only minimal shunt protection to an n-channel device. When a p-channel device is in an n-substrate (p-well technology), the forward resistance is usually much lower and the p-channel FET provides substantial protection to the n-channel FET in its fragile reverse breakdown mode.

III. PULSING ALUMINUM AND POLYSILICON LINES

The transmission line technique has also been used to pulse IC aluminum metal and polysilicon lines, which are found to heat past the melting point before open circuiting, for pulses of about 120 nanosec.

A typical example of the result of a 50 ohm transmission line pulse applied to an Al line (1μm thick, 1213μm long and 4.2μm wide) is shown in Fig. III.1. The line was charged to 220V and the pulse was just barely non-destructive, but some 23μJ were dissipated. Heating caused the Al line's resistance to rise during the pulse (owing to the positive temperature coefficient of resistivity), resulting in the sloped voltage waveform. This almost perfect linear waveform allowed Eq. II.2 to be readily solved analytically to give the 23μJ energy dissipation result. Such an aluminum line, however, requires only

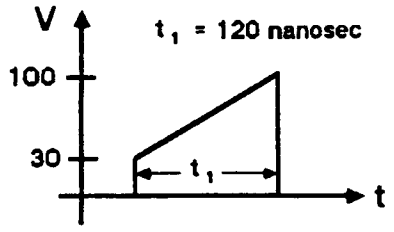

Fig. III.1. Response of a 1213 X 4.2 micron flat aluminum line to a 220V, 50 ohm pulse. Heating causes voltage rise.

about 15μJ to heat past the melting point of 660°C, including heat of fusion. The voltage rises during the entire pulse because the resistivity of Al continues to increase after melting (in contrast to Si; see below). The aluminum line appears to reach at least 1000°C before open-circuiting in one location.

Notice that the 4.2μm wide line can support several amps of current for a considerable period of time (120 nanosec) on the scale of most ESD events. A well-designed ESD protection device will have leadway metal to its pad that is wider than this, and which will support even more current. Metal which is too narrow (e.g., 5 microns) and which crosses over steps can sometimes be the weakest link in a protection device. This kind of metal failure usually occurs in the charged-device ESD test[2], where high currents occur over short periods of time. But leadway metal need only be about 10 microns wide to avoid its being the weak link in most cases.

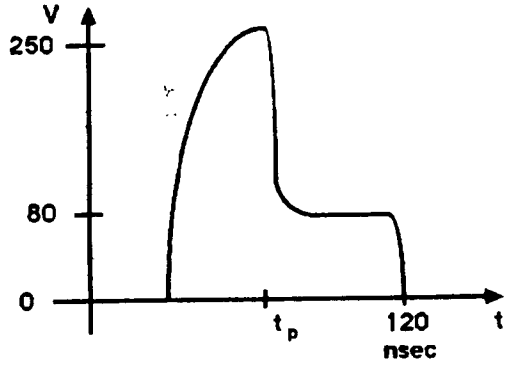

Fig. III.2. Response of a 225 X 9 micron flat polysilicon line to a 1000V, 1 Kohm pulse. Voltage collapses after melting.

Pulsed polysilicon lines behave somewhat differently, but also melt before open-circuit failure. As shown in Fig. III.2, the voltage waveform rises and levels, then falls sharply to a sustaining value. The pulse source used here is 1000V with 1 Kohm internal impedance (technique is explained in Sec. IV). The energy absorbed by t_p is sufficient to melt the silicon completely, whence the voltage drops due to the lower resistivity of molten silicon. This 1000V pulse was destructive (open circuit in one location) to the 225 X 9 X 0.5 micron polysilicon line, which measured 500 ohms at room temperature. But the Si melting and voltage collapse can easily be seen, without destruction, for 600V, 1 Kohm pulses to these lines. For these 120 nanosec pulses, the Si temperature must rise considerably beyond melting before the open circuit occurs.

This sort of polysilicon melting can occur in a Mil-Spec ESD test (100 pf capacitor is discharged through a 1.5 Kohm resistor and the device) when the protection device consists of a polysilicon resistor in series with a small NMOS grounded-gate FET. This is not surprising, as the device's R-C waveform in the Mil-Spec test resembles the transmission line pulse. However, the large initial voltage produced by the Mil-Spec network is often enough to fail the device by blowing out the field oxide near the pad, a failure mechanism not seen with the 1 Kohm transmission line pulse. The reason for this appears to be high initial current driving ability of some Mil-Spec networks, traceable to parasitic capacitance across the 1.5 Kohm resistor. The result is a high initial voltage, sufficient to blow out the field oxide at the high field point on the poly resistor, nearest the bond pad. This concept was confirmed by another transmission line experiment, where this "first-contact" failure mechanism was seen on the same 500 ohm poly resistor as discussed above, using a 350V, 25 nanosec pulse with 25 ohms impedance.

The field oxide breakdown seen on poly resistors has a very unusual behavior. As soon as the applied voltage exceeds the dielectric breakdown voltage of the oxide under the poly (350 - 600V), a leakage path is established to the substrate. This occurs at the location of the peak electric field, i.e. the first contact. Any subsequent zap erodes the polysilicon around the damaged oxide. The damaged oxide gets isolated, and the previous electrical damage is healed. Frequently one zap will cause both the oxide damage and the erosion of the poly. In this case no damage can be seen electrically, but a high power microscope shows poly erosion. Eventually the entire contact erodes, giving an open circuit. The erosion of poly in the contact can also be accompanied by damage to the overlying passivation. In summary, polysilicon resistors are subject to dielectric breakdown under the first contact if ESD voltage exceeds 350V; the damage is cumulative and is not always detected electrically until the contact becomes an open circuit.

IV. NMOS FET BREAKDOWN

Most ESD protection devices in MOS integrated circuitry involve the operation of n-channel MOSFETs in breakdown mode, often called snapback because the drain-source voltage drops in the high current regime. Various numerical models and experimental studies of NMOS snapback have been done[3,4]. Here we will discuss the results of four-terminal high current i-v characterization of MOSFETs, using the basic transmission line pulsing method along with several extensions. The results relate to the localization of snapback current in NMOS FETs ("lock-on"), recently observed by these authors using an infrared microscope[1], and to the physical details of snapback itself.

The transmission line pulsing scheme is ideal for observing the high current (up to several amps) snapback region of a MOSFET, with non-destructive 25-150 nanosec pulses observed on a storage oscilloscope. This technique was used (1) to show that the differential resistance of an NMOS FET in snapback is lower than that of a typical forward biased p-n junction, a result that affects CMOS ESD performance.

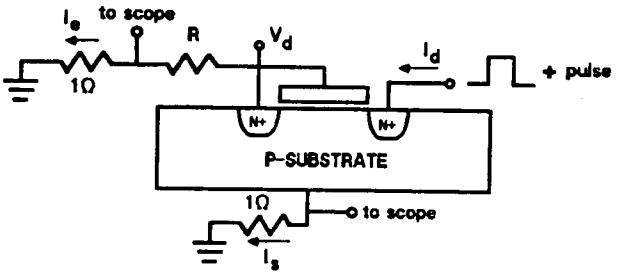

Fig. IV.1. Scheme for monitoring NMOS FET source and substrate currents. Transmission line pulse is applied to drain.

The source and substrate currents during an NMOS breakdown pulse can be monitored to find the constituents of the total snapback current. The measurement scheme is shown in Fig. IV.1. Resistors are used to determine the current constituents and to induce a positive voltage on the source. Emitter (source) current always dominates in our LDD NMOS FETs, but substrate current exists and is essentially constant with respect to variations in a positive source-substrate voltage. Thus, snapback conditions in the intrinsic FET are not changed by altering the backgate voltage, in agreement with Ref. 4.

The voltage waveform that develops across a MOSFET in an actual ESD event is a complicated one, often oscillatory, including both forward and reverse bias of the device. Any memory effects that exist on account of, say, a forward bias being immediately followed by a reverse bias are of interest. Such effects can be studied in their base form with the transmission line scheme shown in Fig. IV.2. The diode in the polarized matched load is replaced by a diode-transistor circuit with memory (triggered load), which produces on the device (with less than 50 ohms resistance) the "bipolar" double pulse as shown. The triggered load stands off the charging voltage, reflects the first pulse, and terminates the second pulse with a matched load when the npn transistor is triggered by the capacitor. During the first reflection this capacitor is discharged by the pnp transistor, yet the load resistance on the transmission line is high at that time, as desired.

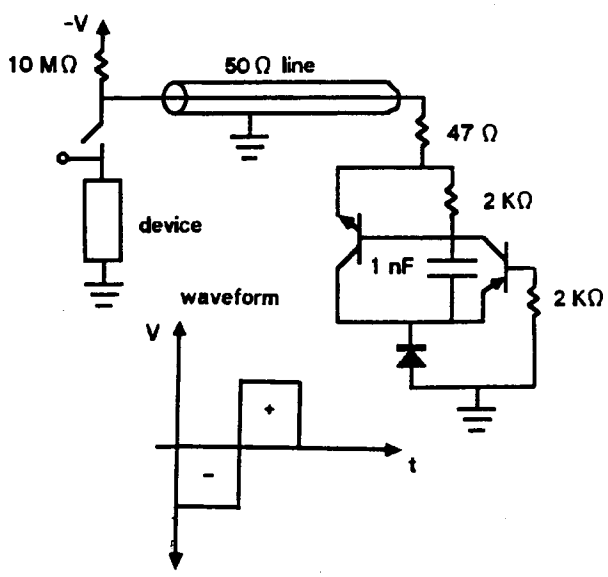

Fig. IV.2. Transmission line with triggered load, producing a bipolar pulse for observing memory effects.

In the case of NMOS FETs, this technique was used to learn that a forward bias followed by reverse bias to the drain will significantly raise the destruction energy. The effect is evidently due to charge storage in the substrate during the forward bias pulse; this charge is uniformly distributed and serves as the seed current for buildup of the avalanche current in reverse breakdown. Such conditions allow for more uniform distribution of the reverse breakdown current than if the seed current originated at local high field points.

Other charge storage effects can be seen under these conditions when the first pulse beneficially charges a floating node. For example, when an n-well CMOS inverter output (refer to Fig. II.3a) is pulsed with respect to Vss (substrate) while Vcc (well tap) floats, an initial negative charge induced on Vcc over entire chip will serve as base current for the vertical pnp transistor when the positive pulse hits, and thus protect the vulnerable n-channel FET with a low resistance path. Again, the effect of an alternating voltage is to increase

the ESD destruction energy. These effects were most easily studied with 50-100 nanosec pulses, as we used inexpensive bipolar transistors. Careful construction of a high-speed triggered load with fast transistors would allow study of these phenomena on a shorter time scale.

Full i-v characterization of a MOSFET, including the snapback region and the effect of gate and substrate voltage variations, is possible with another pulsed technique that avoids the steep load line of a pure 50-ohm source. A resistor (e.g., 1 Kohm) is put in series with the charged 50-ohm coax line and the device, to give a high impedance pulse source. Unwanted reflections are suppressed by a shunt 50 ohms at the same location (Fig. IV.3). FET i-v curves can thus be determined under pulsed conditions, and device behavior in the snapback region can be seen.

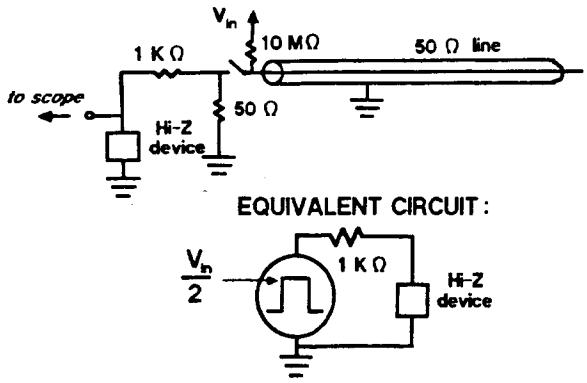

Fig. IV.3. Using a 50 ohm transmission line to produce a reflection-free pulse source with high internal impedance.

Using this technique NMOS snapback sustaining currents are found to scale only weakly with device periphery, a result to be expected from our previous IR microscope observation of current "lock-on"[1], whereby snapback current is confined to a fraction of the device periphery. Fig. IV.4 illustrates how the sustaining current (not always reproducible) is observed. An oscillation is seen when the high impedance load line intersects the device i-v curve in two places. Because the sustaining current is difficult to predict, arguments about CMOS inverters with p-channel load characteristics incapable of reaching the n-channel sustaining current[4] are questionable. However, it is possible to add ballast resistance to the NMOS FET to inhibit current confinement[1], under which conditions the sustaining current should be more predictable.

The high impedance pulsing scheme is also used to characterize high resistance ESD structures, e.g. many input protection devices with a series resistor of several hundred ohms. Note that if the 1 Kohm resistor is deleted, a pulse

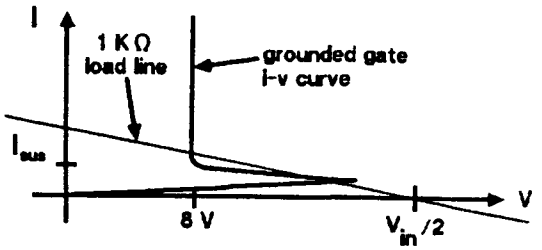

Fig. IV.4. Measuring the NMOS snapback sustaining current with 1 Kohm pulses. Oscillations result when device i-v and load line multiply intersect.

source with more current driving ability results, one which is reflection-free as long as the device's resistance is high compared to 50 ohms. Here the objective must be to observe destruction rather than to plot i-v, as the device voltage is always $V_{in}/2$.

V. OTHER TRANSMISSION LINE PULSING TECHNIQUES

Infrared microscope observations of FET current distribution (see also Ref. 1) were made using a technique that allows repeated transmission line pulses to be applied to a device. A power FET is used to ground a charged transmission line through a device, its gate being triggered by a steady stream of pulses (Fig. V.1). The 2 μf capacitor allows smooth loading of the power supply, while the 100K resistor prevents the power FET T_1 from having its drain-source capacitance charged through the device.

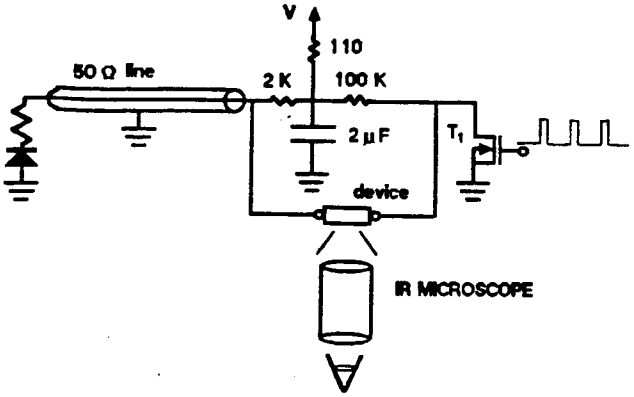

Fig. V.1. Technique for repeated transmission line pulsing, allowing IR microscope observations.

The basic transmission line pulsing scheme can also be extended to allow pulse measurements at the wafer level by using a coaxial probe, as shown in Fig. V.2. The device (still presumed to have less than 50 ohms resistance) is now on wafer and is contacted by the center of the coaxial probe and a ground probe; the ground returns to the coax shield by a short loop of wire. Only the section of line l_1 is charged, and the signal appearing on the device is the same

regardless of the length of l_2. If the scope probe is located as shown a reflection from l_2 is seen first, followed by the usual voltage-divider relation appropriate to device resistance R_d. Things can be observed in this convenient fashion if l_2 is less than l_1, but in all cases l_2 serves only as a conduit for the incident and reflected pulses.

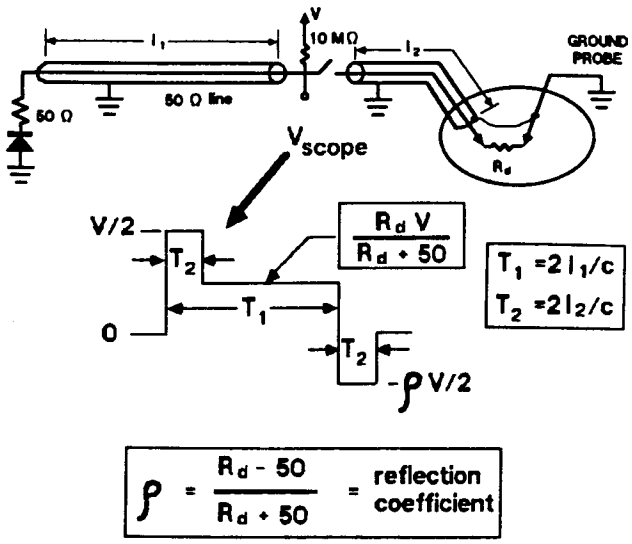

Fig. V.2. Wafer level transmission line pulsing scheme, using a coaxial probe. Length of feed line l_2 does not affect device waveform.

The wafer level ESD characterization technique allows the whole range of transmission line measurements to be made. Even the high impedance measurement can be done by outfitting a coaxial Kelvin probe with an appropriate voltage divider network of chip resistors. By examining the destruction energy for long and short pulses (ranging from 10-150 nanosec), one can get a fairly good idea of how the device will perform under human body and charged device ESD tests when packaged.

VI. CONCLUSIONS

The major conclusions of this work are

i) Transmission line pulsing (TLP) produces brief, high current pulses that simulate various features of ESD waveforms. Pulse length and internal impedance are adjustable, and unwanted reflections can be suppressed. As the pulses and the device response are analytically describable, i-v curves and circuit models appropriate to the current and time scale of ESD can be developed. In this way TLP performs the functions of a curve tracer in an otherwise inaccessible region of the current-voltage plane.

ii) Flat aluminum and polysilicon IC lines, when pulsed by TLP on the 100 nanosecond scale, absorb enough energy to melt, often non-destructively, before failing by open circuit in a single random location.

iii) TLP has shown that NMOS FETs generally have lower resistance, and greater vulnerability to damage when ESD pulsed, than do PMOS FETs. Thus the NMOS FET is the weak link in a CMOS output. In a study of the four-terminal NMOS FET i-v relations in the snapback region by TLP, the substrate current was found to be insensitive to backgate voltage, and the snapback sustaining current was unstable due to localized current flow.

iv) A special TLP technique for studying memory effects showed, with a bipolar pulse, that charge storage in an NMOS FET during forward bias can guard against destruction by a reverse breakdown pulse that immediately follows.

v) Extensions of TLP for ESD include a repeated pulsing scheme for observing device current on an infrared microscope, and a technique with coaxial probes for doing ESD tests on protection devices at the wafer level.

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