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Designing power supply clamps for electrostatic discharge protection of integrated circuits

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Abstract

Power supply electrostatic discharge (ESD) clamping is needed to protect the IC power supply as well as to provide convenient discharge paths for ESD currents, and thereby simplify the total design problem. A variety of methods are reviewed and explored, notably those employing diodes or field effect transistor (FETs) built in bulk complementary metal-oxide semiconductor (CMOS) technology and avoiding avalanche behavior. Power clamping can occur across comparable power supplies or between a power supply and ground; there are diode and FET methods for each. Designs extend to clamping for mixed voltage supplies on a single chip, including power supplies above the gate oxide tolerance. New designs and results for power clamps based on PMOS FETs are presented for the first time.

1. Introduction

To protect an integrated circuit (IC) product against electrostatic discharge (ESD), the designer must first consider the various stresses to which the component will be subjected in qualification testing and in actual handling. The standard ESD tests which best simulate actual handling conditions include the Human Body Model (HBM) [1, 2], the Machine Model (MM) [2, 3], and the Charged Device Model (CDM) [4, 5], all of which involve multiple current paths through the device. A protection scheme for a product includes both local and global elements, as each pad must be used as an entry or exit point for ESD current, and the current must also pass harmlessly through the rest of the chip somehow. This paper will focus on protection methods for the complementary metal-oxide-semiconductor (CMOS) IC, with an emphasis on CMOS ICs built on a p-type substrate. In particular, we will describe designs relating to defined ESD current paths from one on-chip power supply line to another as part of global protection. Also, we will show how the local and global protection of an IC link up to allow components to pass the standard ESD tests and survive ESD events during their lifetime.

The design process for ESD protection of an IC may begin with local protection at each pad. The most common protection method for input-only pins uses dual diodes as shown in Fig. 1. This is a two-tiered dual diode structure, with much smaller diodes D3 and D4 protecting the input buffer following a resistor R that is typically 100–200 ohms, or higher if speed is not critical. Most of the ESD current passes through the large diodes D1 or D2, one of which will forward bias depending on the polarity of the ESD pulse. It is well known that the forward-biased diode is a very robust ESD protection device which, if laid out correctly in a well-designed process, will pass a large ESD current per unit area with low voltage drop, without damage [6]. Thus the dual diode structure can form the first step of the desired smooth ESD current path through the chip.

Indeed, many designers use (what might be called) the dual diode principle as much as possible in their chips. For example, a typical CMOS input/output (I/O) pad such as in Fig. 2 has driver devices T1 and

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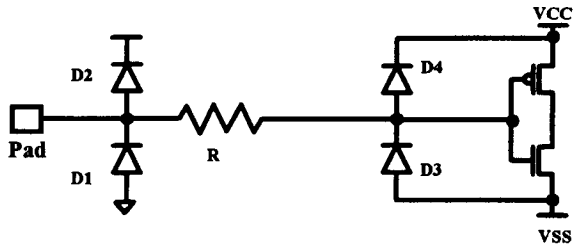

Fig. 1. Dual diode method for protecting an input buffer.

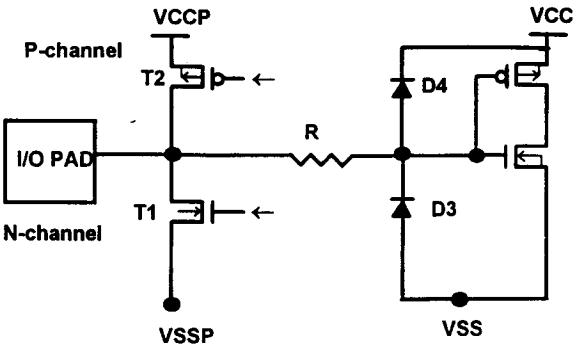

Fig. 2. CMOS input/output buffer protection. T1 and T2 have built-in parasitic dual diodes which can be enhanced through layout.

T2 which have parasitic diodes to power and ground resembling the D1 and D2 diodes of Fig. 1. Even though the NMOS T1 FET might have its source on a separate Vssp supply as shown in Fig. 2, its D1-like diode to Vss (substrate) is a particularly good one if the CMOS process is on epitaxial silicon with a conducting p+ substrate (the emphasis in this paper is on this kind of IC technology). This diverts most of the current in one polarity of ESD pulse. The other polarity is steered toward T2's inherent D2-like diode to Vccp, which can be optimized (or even augmented) through obvious layout methods. Thus, the designer avoids much current being handled by the breakdown mode of the NMOS T1 device. In recent years, the NMOS device has become weaker and weaker in ESD due to self-aligned silicide (salicide) on the drain and source, and also because of lightly-doped drain (LDD) structures. Even when salicide is blocked between drain and gate with a section of *n*-well [7], it is best to use dual diode current steering and avoid much breakdown current flowing through the T1 transistor during ESD. For that reason, dual diode methods are commonly used on outputs as well as inputs.

The scaling of power supply voltages below 5 V in recent years has meant that components need to be backward compatible, to some extent, with chips running on higher voltage supplies. Fig. 3 summarizes how this problem breaks out into high-voltage tolerance and high-voltage drive, and how high-voltage tolerance (of input signals) depends on whether or not the high voltage appears on the chip as a reference. The dual diode principle can be used for self-protection of all outputs, inputs, and I/Os where there is a high-voltage rail of this kind, because there can be a D2-like diode from pad to that high-voltage rail. Table 1 summarizes the situation with four typical CMOS IC processes of the past few years, with Proc1 being the last of the processes allowing a continuous 5 V across the gate oxide. Various issues surrounding mixed-voltage interfaces are discussed in other references [8, 9].

The foregoing covers all the input and output pins for many products, especially digital ICs. Sometimes a pin needs to be raised above the power supply voltage, as when test modes are triggered with EPROM address pins [10], and a dual diode approach is not appropriate. Also, some analog ICs have special requirements which rule out dual diodes. For these pins, an NMOS FET, a silicon-controlled rectifier (SCR), or thick field oxide (TFO) device is better to use. A tremendous amount of effort has been spent on improving the ESD hardness of such devices, with new reports appearing every year in professional journals and in the Proceedings of the EOS/ESD Symposium. But

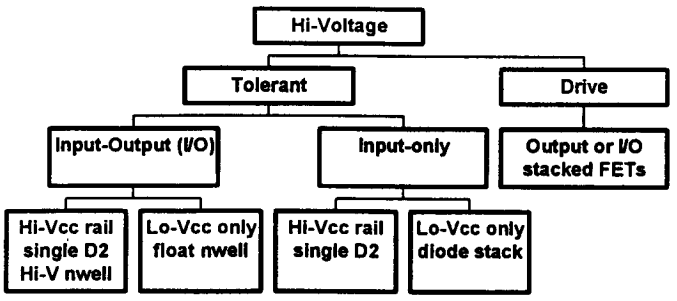

Fig. 3. Classification chart for high voltage input or output pins.

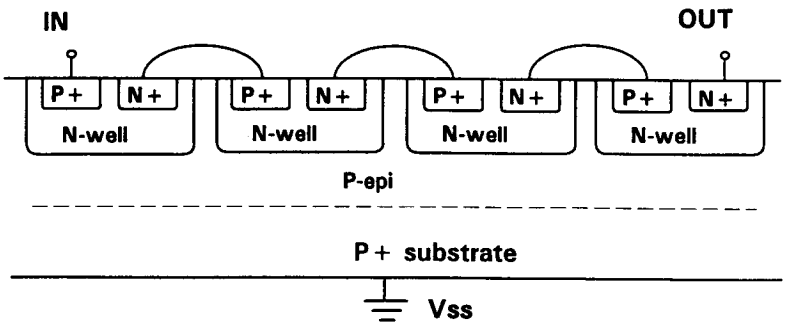

Fig. 6. Cross-sectional view of 4-stage diode string in p-substrate CMOS.

2. Diode and bipolar clamps

Diodes are commonly built in floating n-wells in p-substrate CMOS and are actually pnp transistors because the common substrate acts as a collector (see Figs. 6 and 7). We will begin with straight diode string ESD clamps between power supply pins [13–15], called bridging diodes (Fig. 8).

2.1. Bridging diodes

Fig. 8 shows (plain, unbiased) bridging diode clamps between peripheral and core power supplies. The single diode on the Vss clamps is, of course, the n+ junction on the p-substrate, while the stack of four is a diode string cell. Also shown in Fig. 8 is a typical diode string between Vcco and a core Vcc. Notice that the Vsso–Vss arrangement is bidirectional (because of the parasitic diode), while the Vcco–Vcc coupling is unidirectional, in agreement with the notation in Fig. 4. Both kinds of strings help complete the current path for the various pin combinations required by HBM and MM, but the Vsso–Vss diode strings are especially important as charge couplers from substrate Vss to output circuitry for CDM [16].

The number of diodes in a clamp intended to connect power supplies of identical nominal voltage is set by the desired noise immunity level, and four diodes was a typical upper limit on 5 V chips. Two or three diodes is more typical on chips with lower supply voltage. But if the two power supplies are of different nominal voltages and the diodes are expected to support a voltage difference in steady state, the full leakage vs temperature and voltage behavior must be understood.

As described in Refs. [8,9,13–15], the diode string's pnp gain results in loss of forward current to the substrate, especially at high temperatures, thus reducing the voltage across downstream diodes and increasing the current requirement for a given voltage. Also, the pnp chain amplifies junction leakage of the downstream n-wells. Ref. [13] shows that the basic diode forward voltage V_f at Kelvin temperature T_1 at a given current can be calculated from the forward voltage at reference temperature T_0 as follows:

$$V_f(T_1) = nE_{g0} + \left(\frac{T_1}{T_0}\right)\left(V_f(T_0) - nE_{g0}\right), \quad (1)$$

where $E_{g0} = 1.206$ V and n is the diode ideality factor. The temperature coefficient of V_f will thus be negative,

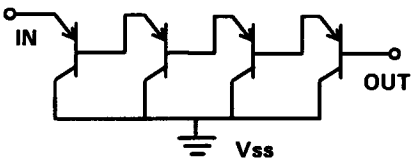

Fig. 7. Darlington-connected pnp transistor model for 4-stack diode string.

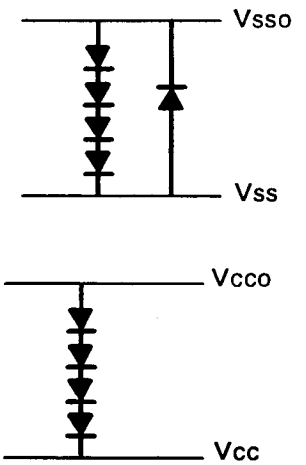

Fig. 8. Typical bridging diode strings between peripheral and core power supplies.

Table 1
Compatibility of submicron CMOS technology; Proc 1 is last 5 V process

5 V	3.3 V	2.5 V	1.8–2.0 V
Proc1	Proc1 low		
Proc2 hi	Proc2		
Proc3 hi+	Proc3 hi	Proc3	
	Proc4 hi+	Proc4 hi	Proc4

many IC products can be designed with some kind of dual diode at every pad, as discussed earlier. This completes the local element of the design process; what remains is the global element. Fig. 4 shows how the entire ESD current flow path through the component needs to be considered. If current is, in this example, expected to pass harmlessly from pad to Vss, we need links first to the Vcc power supplies and then to Vss. While the dual diode in this example provides the link from pad to Vcc1, other structures must provide the other links. Experience has shown that without defined current paths between various power supplies, leakage failure will happen following ESD stress [11–13]. Sometimes new design rules can be formulated so that dangerous structures do not appear in the circuitry, or else the failing structures must be redesigned one by one as failures are noted. Both of these approaches are costly and unsatisfactory in the design factory environment. The ESD specialist does the best job for the customer, the IC product designer, by allowing the freedom to design a wide variety of circuits and layouts allowed by process design rules, then assures that ESD protection occurs through application of a few critical cells specified by the ESD designer. This paper is aimed at reviewing the various methods for providing ESD links among the power supplies so that ESD current can pass harmlessly through the chip for all ESD stresses and tests.

The various kinds of power clamps can be classified according to function as shown in Fig. 5. These are generally either bridging clamps (as between Vcc1 and Vcc or Vss1 and Vss in Fig. 4) or stand-alone clamps (as between Vcc and Vss). In the following sections we will explore the elements of this chart, but for those discussions it is more meaningful to observe the differences in construction of the clamps. Accordingly, we will explore diode and bipolar clamps first, followed by FET clamps.

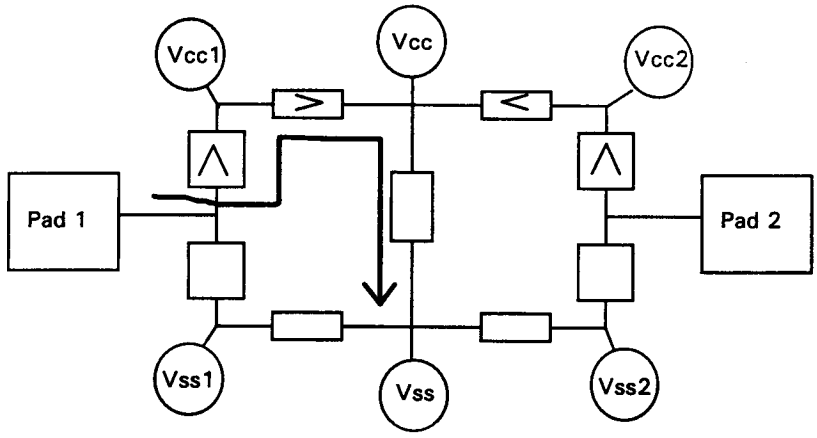

Fig. 4. Example of preferred ESD current path from one pad to another, showing passage through I/O circuits and power supply

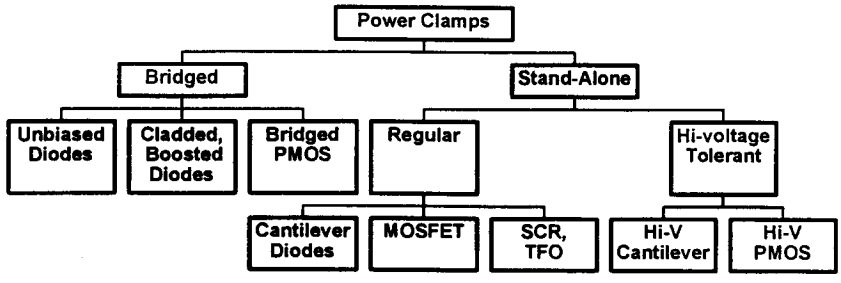

Fig. 5. Classification chart, by function, for power supply clamps.

around −2.2 mV/K for typical conditions, and diode leakage will increase at higher temperatures.

When the pnp current gain β of each element of a diode string is considered, the total voltage dropped across a number m of identical diodes is

$$V_t = mV_1 - V_0 \log(\beta + 1)\left(\frac{m(m-1)}{2}\right), \quad (2)$$

where $V_0 = \ln(10)(nkT/q)$, 60 mV for an ideal diode at room temperature. V_1 is the base–emitter voltage for one diode (collector and base shorted) at emitter current I_1. For the moment we neglect series resistance and variations in β. This can be shown to be a special case of

$$V_t = mV_1 - V_0\left(\sum_{i=2}^{m} \log\left(A_i(\beta_{i-1} + 1)^{m-i+1}\right)\right), \quad (3)$$

where A_j is the normalized area (i.e. $A_1 = 1$) and β_j the current gain of the jth diode in a string. Full details are given in Ref. [13]. When β is constant (as with low current leakage conditions), note that an area taper (A_j growing smaller as j increases) helps to increase the total voltage supported by a given current.

An ESD path through a diode string causes high current density and its associated effects on diode series resistance and β. Ref. [13] describes how to model diode strings with a simple Ebers–Moll transistor model, including proper treatment of the decline of β with current density (Webster effect [17], Fig. 9). Diode performance in the ESD current regime is usually optimized by having long, tightly packed, minimum width n+ and p+ stripes, fully contacted and metallized. Diode behavior can then be predicted on a per unit length basis for a particular process and associated design rules, where the length of fully surrounded diffusion of one kind measures the size of the diode. Transmission line pulsed (TLP) I–V [18] results

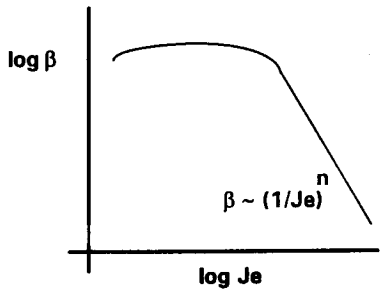

Fig. 9. Log of current gain vs log of emitter current density for a typical diode string pnp transistor, allowing simplified modeling of the diode string performance. The coefficient n is measured for each process.

for one example of tapered four-stack diodes in a 0.35 μm technology are shown in Fig. 10, with current per unit area given.

Let us return for a moment to the leakage current regime of diode strings sustaining a small forward voltage. Because of current loss to the substrate, the latter stages will suffer an incremental voltage decline unless there is a taper in diode area, as described by Eq. (3). While tapering can minimize leakage, it is not compatible with maximizing ESD performance because of series resistance and declining beta. A method to improve leakage behavior over temperature without affecting ESD performance at all is to augment the diode string with a bias network to distribute small but significant forward current to the diodes. Ref. [13] proves mathematically how best to do this; it is almost exactly correct to remember that equal current through each diode produces the most voltage for a given current. The diodes in Fig. 11, sometimes called cladded diodes, support extremes of 5 V and 3.3 V power supplies. They are biased with megohm-range resistors (realized as long-channel PMOS FETs in p-substrate

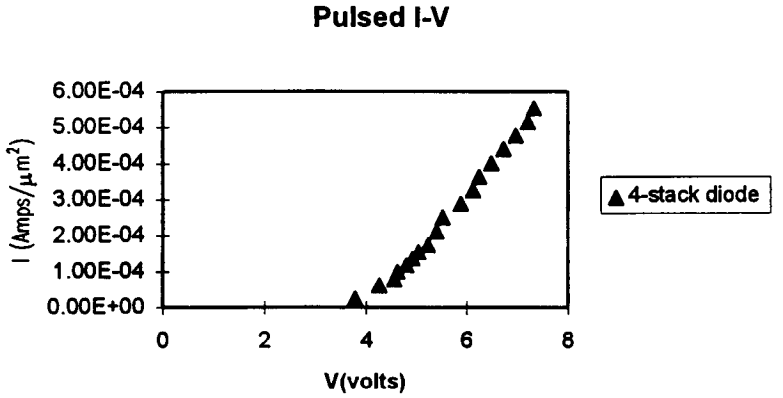

Fig. 10. Normalized pulsed I–V for 4-stack diode string in 0.35 μm technology.

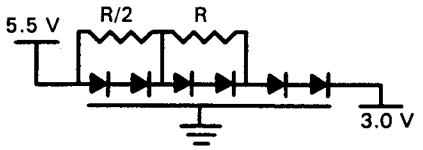

Fig. 11. Bias network for a 6-diode mixed power supply clamping string, designed to minimize leakage current at high temperature.

CMOS), ratioed so that they distribute equal current at each tap, assuming that most current is lost to the substrate because of β. The result is that high-temperature leakage performance can be substantially improved, costing only a submicroamp background current at low temperature [13]. There also are simple active circuits to supply current only when needed so that the low temperature background current can be largely eliminated [13, 19].

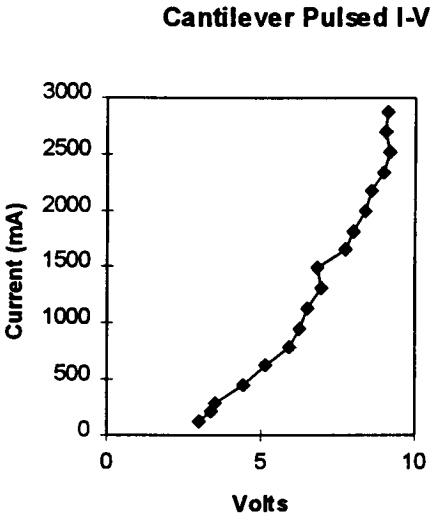

Fig. 13. Cantilever clamp pulsed I–V for high beta process.

2.2. Cantilever diodes

Because of the current gain at each stage of an n-stage diode string, the current at the output is a factor of $(\beta+1)^n$ less than the input current. Thus, even for a fairly low β, the majority of the current flows to the substrate. It becomes possible to consider alternatives to attaching the output to another power supply if some kind of small circuit can sink the remaining base current. This would give a stand-alone power clamp and free the user from assuring that the two power supplies always track within the voltage limits. The concept of not having a power supply anchorage at the far end of the diode chain has come to be known as cantilevered, or cantilever, diodes [13, 19].

Fig. 12 shows the schematic for a cantilever clamp which uses a PMOS FET T1 of about two hundred microns gate width to sink base current. Other transistors are long channel, such as the RC timer resistor T2 and the anti-leakage bias FETs. Note that the bias FETs are not needed to sustain any permanent diode voltage drop, but are there to supply high temperature leakage current to floating wells. This avoids amplified leakage current and possible thermal runaway. The RC-timed T1 gate has a time constant in microseconds, long enough to clamp ESD events but short enough that total charge sunk is small compared to what batteries and power supplies can provide for powerup. The current sinking transistor, T2 in Fig. 12, need not be PMOS; indeed a smaller NMOS FET (50 microns has been used successfully) following a small inverter can be comfortably packed into a small area.

Fig. 13 is a pulsed I–V curve of a rather good cantilever clamp, one built on a high-β (>10 at low current) flash erasable programmable read-only memory (EPROM) process whose power supplies are also voltage tolerant slightly beyond 12 V. Thus there is plenty of voltage headroom to allow the startup voltage of 6 forward-biased diodes. Note that this cantilever clamp can itself (in the size of about two bond pads) sink far more than the peak current in a 4000 V HBM pulse and still be well below the danger voltage. In the years since the cantilever clamp was developed and first used, flash EPROM products have made heaviest use

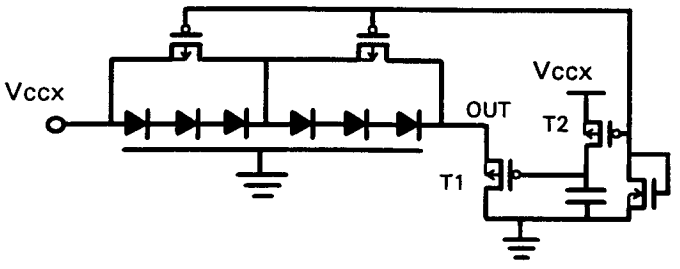

Fig. 12. Six-stage cantilevered diode string with resistive bias network and termination circuit.

of it for several reasons: flash processes tend to have high pnp β, they have voltage headroom because of 12 V programming, and for that same reason they have thicker p-channel oxides and longer p-channel gates, reducing the advantage of the PMOS power supply clamps we are about to discuss.

The success of cantilever clamps on flash EPROM products also led us to use them on flash Vpp programming pins, with modified circuits. Vpp is a rare example of a pin that can use a cantilever clamp while not being a power supply pin in the traditional sense. Nonetheless, the need to toggle Vpp in an EPROM product is limited enough that accompanying circuits could be designed easily. A detailed discussion is now in the literature [20].

2.2.1. High-voltage cantilever clamp

The cantilever clamp modified for 5 V tolerance on a 3.3 V process [20] is shown in Fig. 14. ESD current sinking is exactly the same as for an ordinary cantilever clamp. The special feature of this circuit is that the long-channel devices T2 and T3 establish bias point v3.6 at no more than 3.6 V, which keeps oxide voltages low with minimal leakage current from Vccx to ground. T4–T6 bias the diodes weakly and thereby drop much of the excess voltage. T1 is thus held subthreshold (current being limited by T4-T6) while T2 and T3 also leak to ground a minimal (submicroamp) amount because they are long channel devices with gate and drain attached. In this way, a power supply clamp with the same ESD performance as one tolerating only the low gate voltage is achieved with very little extra area, about 5%.

More information about the 5 V-tolerant cantilever clamp is in Refs. [20,21]. This clamp turned out to be an interim solution for low-voltage p+ substrate CMOS logic processes at the 0.6 μm stage for several reasons. As CMOS processes and devices advanced from 5 V to 3.3 V and below, the pnp β declined, as did the danger voltage on pulsed Vcc and associated voltage headroom available to power clamps. At the same time, device dimensions including gate widths kept on shrinking. This made for more compact diodes, but the net effect was to point in other directions for power clamps, to be discussed below.

2.3. SCR and other bipolar clamps

Sometime in the 1980 s, semiconductor ESD protection designers began to consider Vcc to Vss protection seriously. Until that time, there was often only one power supply line on a chip, probably with substantial capacitance, and with the likely ability to self-protect through distributed nondestructive breakdown events. For bulk NMOS IC technology, more common than CMOS until the mid-1980 s, Vcc could break down through NMOS snapback [22] distributed across the entire bus, usually harmlessly. Until the mid-1980 s, research on ESD protection was mostly concerned with protecting the input and output devices properly, and no pattern of power supply failure mode was widely noticed or reported. Then with widespread use of CMOS, the Vcc–Vss protection was presumed to be continued npn snapback, or perhaps distributed and nondestructive SCR latchup with high sustaining voltage. By this time, TLP [18] was being used routinely to inspect pulsed I–V behavior for all current paths through a chip, and ESD workers developed a good feel for the capacitance, breakdown behavior and pulsed voltage danger level for their power supplies.

In 1988 Duvvury et al. [12] discussed power supply protection issues and presented several case histories. Among other things, they described the failure mode of core Vcc to Vss due to close approach of n+ diffusions somewhere in the circuit, which many workers then agreed was becoming a significant hazard, difficult to ignore. Also they noted failures of large internal clock buffers, which, unlike thousands of other internal

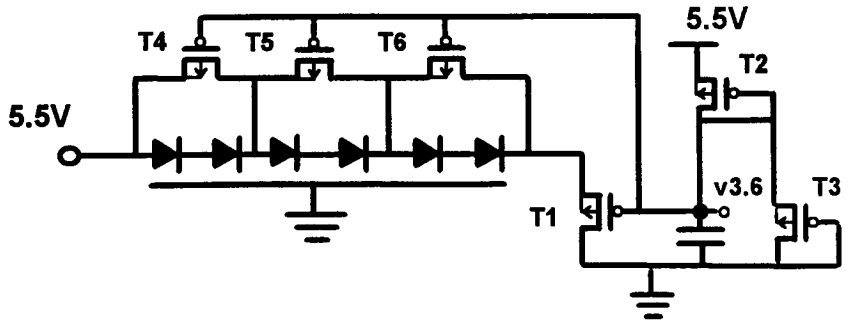

Fig. 14. Circuit model of voltage-tolerant cantilever power supply clamp. T1 is a short-channel device, several hundred microns; the other transistors are long-channel, resistive devices. The node at v3.6 is biased by T2 and T3 to be no more than 3.6 V when the supply hits a maximum of 5.5 V.

inverters on the same chip, could fail because their large size allowed current from several p-channel legs to concentrate in a single n-channel leg. Again, workers at other organizations agreed before long that this was a generic problem. It appeared necessary to enforce more layout rules on design of core circuitry in order to avoid these failures, or else be sure that the ESD current bypassed these hazards. The latter option is executed at lower cost, of course. At this time, the Vcc–Vss protection device of choice (if one was used) was usually the thick field oxide (TFO) lateral npn device, which had been shown to be effective as an input protection device [23, 24]. TFO devices (or the related NMOS grounded gate device) as core and peripheral power supply protection were compact, moderately effective, and rugged as long as the process technology did not have salicided junctions.

In 1993, Johnson et al. [11] discussed some cases where these devices were used to help clamp Vcc to Vss and avoid such events as the aforementioned failure of large clock drivers. But when npn snapback in a TFO or NMOS clamp was competing with npn snapback in a short-channel clock driver, it was difficult to assure survival of the clock driver without redesigning the NMOS section with ESD-hardened longer dimensions as well. By this time, with salicided junctions becoming the norm in logic processes, it was becoming clear that TFO and grounded gate NMOS clamps would become more delicate, and that breakdown devices like these would face a basic triggering problem, as the ESD current would have to flow through them preferentially. The work of Duvvury and Diaz [25] suggested that temporarily coupling a gate voltage to an NMOS FET would help, although their stated purpose was input protection. The challenge of using a salicided NMOS FET with lightly-doped drain (LDD), which had been engineered primarily for circuit performance, for protection of power supplies of any size, appeared to be daunting. But new work was forthcoming.

The SCR has also been used as a power supply clamp. The major issue is not to trigger unintended CMOS latchup during circuit operation. Beginning in 1994, Croft [26, 27] presented a way to use SCRs for power supply protection during ESD qualification and component handling, while then disabling the SCR during product use with an external short. Recently, Ker and co-workers have taken their extensive work on SCR-related ESD protection (see [28, 29] and references therein) to the subject of power supply clamping [30, 31]. Other reports of novel SCR power supply protection [32] have also surfaced.

The work of Tandan [33] provides one final entry in this category of bipolar devices for power supply protection. The author used an RC trigger on a single npn transistor (available in a BICMOS process), employing the npn as a power supply clamp. It was not clear if actual stand-alone pulsed I–V behavior, not measured, could match the published simulations, as the device needs to be very large to conduct amperes of current and avoid the Webster effect [17]. A followup of this study would be interesting.

3. FET clamps

3.1. NMOS and PMOS stand-alone clamps

3.1.1. Clamps for ~~nominal~~ nominal Vcc

In 1993, Merrill and Issaq [34] wrote of using a large NMOS FET (8000/0.8 μm) as a power supply clamp. The gate was driven by a three inverter chain following an RC timer (Fig. 15). The goal of that study was good HBM ESD protection; no CDM studies were done. When Worley et al. [35] studied similar devices and circuits, reporting two years later, they found good HBM power supply protection with salicided NMOS FETs, but failures on CDM. A series well drain resistor was added to prevent CDM damage, but it limited current and the device was considerably larger. Ref. [35] also advocates using a dedicated ESD power line as a central reference point (along with the substrate) for ESD current, possibly even charge-pumping it to allow higher voltage tolerance of inputs for mixed-voltage applications.

Work at our company in this same time period pointed in some new directions, to be published here for the first time. The need for power supply clamping continued, and we needed a successor to the cantilever clamp as processes scaled, voltage headroom disappeared and pnp β vanished. Our rigorous qualification standards required universal application of power clamp cells, meaning that each clamp should pass all standard ESD tests with some margin (>4–8 kV HBM, >1.2 kV CDM) in stand-alone mode, so that an arbitrarily small power supply would be protected. In addition, pulsed I–V behavior must be consistent

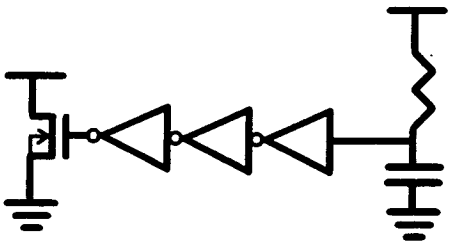

Fig. 15. RC-timed circuit for large NMOS FET power clamp, described by Merrill and Issaq [34].

with sinking at least a 2 kV HBM peak current (1.33 A) below the known danger Vcc voltage for all ordinary circuits in the process, even vulnerable ones (it was expected that every supply would have at least two clamps). These criteria, and the cost-driven desire not to add masks or tamper with the performance-engineered FET process, drove us away from NMOS FET clamps because the salicided devices, even large ones, failed miserably on all ESD tests. Unsalicided NMOS devices resembling Worley's [35] had the same problems with size and CDM behavior.

However, we noticed that the properties of power clamps made from PMOS FETs [36] were quite favorable. Dimensions at or near minimum could be used, so the disadvantage of PMOS current drive per unit gate width over NMOS was hardly noticeable. The PMOS devices (which we will call pmosclamps) in this driven-gate mode were very rugged in all the aforementioned ESD and pulsed I–V tests, sometimes almost impossible to destroy. Yet we did not have to intervene in the performance-oriented process development cycle with wafer splits and such, we just evaluated the process changes as they happened, to confirm continued good performance. As the PMOS FET is free of the positive feedback and negative differential resistance effects of npn snapback [37], it appears to have no difficulty conducting uniformly over a large area, even in the high-voltage breakdown regime. The results to be discussed here are from devices fabricated on 0.35 and 0.25 μm processes, now in manufacturing. Some details of the processes have been released publicly [38, 39].

The basic pmosclamp (Fig. 16) is built around a large (around 3000 μm) p-channel transistor (T1) of near-minimum gate length. Its gate is driven temporarily to ground in two ways. First, a MOS capacitor (C1) helps to overcome the capacitive coupling of the large gate to Vcc. But more important, the inverter driving the T1 gate is heavily weighted toward the NMOS device T2 pulling the T1 gate low with considerable strength. The RC timer formed from T3 (long channel) and C2 sets the time constant (microseconds), much as in the cantilever clamp and others, while the first inverter trip point is set midway between ground and Vcc for high noise immunity.

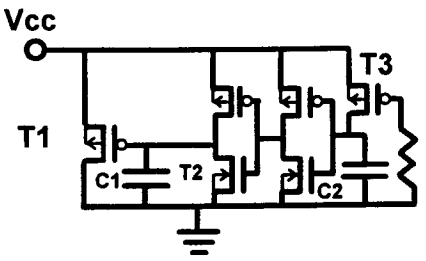

Fig. 16. RC-timed circuit for PMOS FET power clamp (pmosclamp); T2 and C1 enhance gate drive.

Fig. 17 shows pulsed I–V curves for a pmosclamp protection circuit as in Fig. 16, occupying about 7700 μm^2 in a 0.25 μm process. The idealized curve is from a test pattern with the T1 gate artificially hardwired to Vss and shows how close we come to desired grounding of the gate during the pulse. The I–V of a pmosclamp without the optimized trigger circuit including C1 and T2 (data not shown) shows clearly degraded characteristics as the gate does not fully turn on. The gate length used in Fig. 17 matched for the two examples shown, and happened to be well above the process minimum; the pmosclamp now routinely used in products has about 10% higher pulsed current than shown and its gate length is still substantially above the process minimum. The subthreshold leakage of these pmosclamps is not an issue, below 1 μA until considerably above 100°C. The clamps were also shown to be robust against power supply noise, which was simulated on test chips with a high-frequency signal applied to the power supply node. There have been

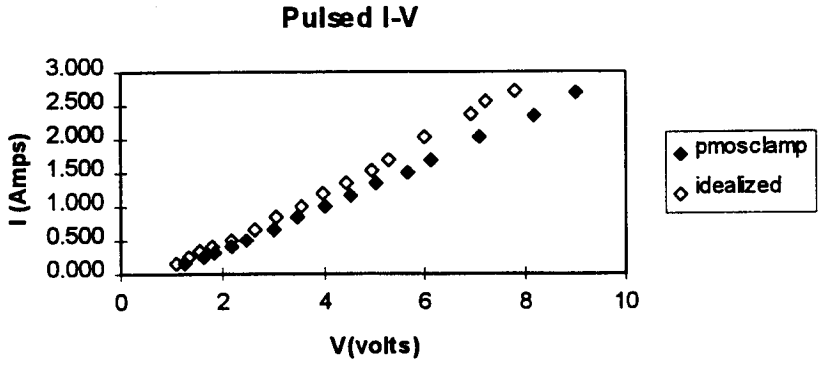

Fig. 17. Pulsed I–V behavior of pmosclamp in 0.25 μm process; idealized curve has T1 gate artificially grounded.

no reliability problems with the clamps on recent products.

Simulations of these circuits (using the standard process MOSFET model) match the pulsed I–V curves almost perfectly to the device model's voltage limit of 4–5 V. Note how the pmosclamp continues to conduct (without destruction) up to 9–10 V, far beyond the observed dc punchthrough voltage, around 5–6 V. Thus the HBM self-protection of these clamps was measured to be 8 kV, and CDM did not fail to the limit of the 2 kV Keytek socketed tester. This is a hopeful sign for CDM protection of products as well; the empirical product results are very good so far. We are now trying to demonstrate the actual time response of the pmosclamp conduction with fast TLP [40].

The equivalent pmosclamp for the 0.35 μm process has roughly the same I–V curve as in Fig. 17, and is in a still-reasonable 12000 μm^2, but this uses over 50% more area than the 0.25 μm process. The trend should continue until such MOS conduction of pulsed currents runs into thermal limits. All of this is because, with shorter FET channels, we can achieve more pulsed and dc current sinking per unit area as processes scale. In the old days of process feature size of 0.8 μm and above, the same PMOS FETs for sinking ESD currents would have been absurdly large; however, just in the past few years, it has become possible to sink more than an ampere of pulsed current through ordinary MOS conduction in a production PMOS FET less than the size of a bond pad. And while devices have scaled dramatically due to Moore's Law, ESD events have not—the human being, source of the HBM, has not scaled noticeably (!), and while electronic packages, source of the CDM, have proliferated into a variety of sizes and shapes, the CDM event is roughly the same as always. Thus, device scaling once again teaches us to be on the lookout for opportunities as well as drawbacks.

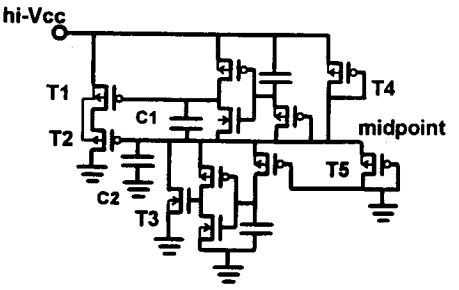

Fig. 18. Circuit for stacked-gate high-voltage tolerant PMOS clamp (vtolclamp). T1 and T2 are large FETs built in the same n-well; circuitry drives their gates low temporarily. T4 and T5 bias the midpoint, rendering dc gate oxide voltages safe.

3.1.2. *High-voltage tolerant FET clamps*

For compatibility with signals from chips with earlier-generation power supply voltage, we want to enable an on-chip power supply Vccx, greater than the voltage that can be safely applied for long-term reliability to a gate oxide in the process. As discussed earlier, clamping of this kind of supply can be done by bridging it to core Vcc via a diode string or a pmos-bridge clamp (next section). But as in the case of the cantilever clamp, a stand-alone solution is often desired, allowing Vccx to be on when Vcc is off. This is allowed with the stacked pmosclamp (vtolclamp) as shown in Fig. 18. There are two large (about 4000 μm in the 0.25 μm process) p-channel devices in the same n-well, with no required contact to the common node, thus allowing tight layout. The midpoint voltage of approximately Vccx/2 is set by long channel devices T4 and T5. This reference voltage allows only Vccx/2 to be dropped across any of the gates in the circuit. The trigger circuits were modeled after those in the pmosclamp, where the capacitors and NMOS FETs pull the gates as low as possible and RC circuits time it out.

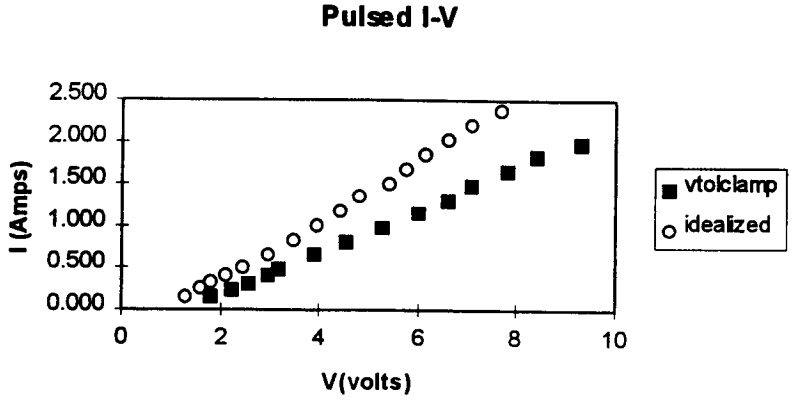

Fig. 19. Pulsed I–V of vtolclamp in 0.25 μm process. Idealized curve has T1 and T2 gates artificially grounded.

The ESD and TLP (Fig. 19) performance of the vtolclamp was on par with the pmosclamp for both the 0.35 μm and 0.25 μm processes, with device sizes scaled similar to the pmosclamp as described earlier. About twice as much area was used for the vtolclamp due to conservative layout and circuit design. Prospects are good for compaction of the layout and for use of more aggressive circuits, improving the current per unit area of the vtolclamp in the future by perhaps 30–50%.

Worley et al. [35] also described clamping high voltage power rails with stacked FETs; PMOS devices were described in one example of clamping their Vesd, the dedicated ESD power bus. Their reference voltage on the lower gate was a low voltage Vdd supply, which provided large capacitance to ground.

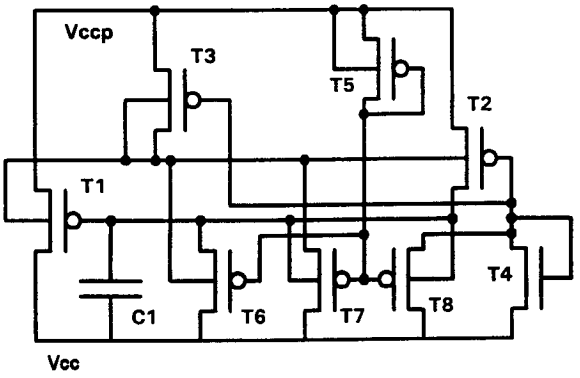

Fig. 20. Circuit for pmosbridge clamp, intended for (peripheral) Vccp voltage greater than (core) Vcc.

3.2. PMOS bridging clamps

Earlier, we treated the case of mixed voltages on a chip, where bridging diodes clamped two separated supplies of differing voltages, for example, Vccp to Vcc. There is a pmos-based version of this [36] that can be more efficient than diode strings; the circuit for this (called the pmosbridge) is shown in Fig. 20. The large PMOS clamp transistor T1 is built in a floating well, and its gate is timed on and off by the RC network formed by long-channel T2 and C1. The rest of the transistors are small devices that pull the n-well and T1 gate to the proper voltage following a transient. The usual clamp mode will be Vccp higher than Vcc, where, after the RC time constant, T2 pulls the T1 gate to Vccp and T3 pulls the n-well to Vccp. Meanwhile, T5 holds T6–T8 off. In the event that Vcc is temporarily above Vccp (as can happen during powerup), there is no attempt to clamp the core Vcc, but T6 and T7 will pull the T1 gate and n-well high, shutting off T1. T8 assures that there is no threshold drop across T4, so that T3 turns off completely. This way there is no long term leakage irrespective of which of Vccp and Vcc is higher.

One version of the 0.35 μm process can tolerate 3.3 V gate voltages, and occasionally has 5 V rails on the chip. Such a 5 V power supply could be clamped all the way to ground by the vtolclamp, bridged to 3.3 V by a string of 6 diodes, or bridged to 3.3 V by the pmosbridge circuit. Fig. 21 compares the current per unit area sunk by a pmosbridge to a 6-diode string in this process, showing the advantage of the pmosbridge. However, remember that the 6-stack will also pass some current to Vss because of the vertical pnp β effect, leaving less for Vcc to sink. Even so, the pnp β effect is fairly weak in these deep submicron processes. The bridge clamps are best used when core Vcc is large and highly capacitive, so that the current path to

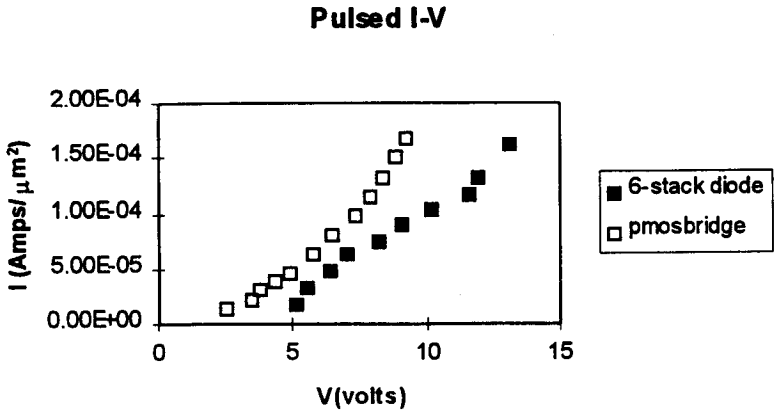

Fig. 21. Normalized (current/μm^2) pulsed I–V of pmosbridge compared with 6-stack diode, intended for 5 V–3.3 V bridge in 0.35 μm process.

ground will not develop much additional voltage. Otherwise, the stand-alone vtolclamp is the best option for a high voltage supply.

4. Summary

Power supply clamping has become important for ESD protection for a variety of reasons. First, power supplies in IC products can have their own special ESD weaknesses, as when internal buffers become too large or when n+ diffusions on unlike power supplies happen to approach too closely. Power supply protection can be forgiving of these layout-related weaknesses, with substantial lowering of design costs.

Power supply clamps are best used as part of a global, modular approach to ESD protection of IC products, and help result in a well-defined current path for each ESD event in stress testing or actual handling. Coupled with the p + n+ diodes available in CMOS processes, power clamps can often allow all significant current paths to avoid avalanching junctions completely. Thus, the ESD designer finds a way to become largely unconcerned with the details of process development, and thereby renders a cost-saving service to the organization.

The various kinds of power supply clamps can be classified by function as shown earlier in Fig. 5. Power clamps can bridge comparable Vcc or Vss supplies, or they can provide stand-alone clamping from power to ground. Various methods can be used to clamp power supplies which sustain high dc voltage; i.e. voltage beyond the dc voltage sustainable by the gate oxide. The devices used to accomplish power supply clamping are varied. Historically, these first clamps tended to be adapted input protection devices like TFO, grounded-gate NMOS FETs, and SCRs, as well as diode strings adapted from dual-diode protection devices. Later on, diode strings were improved through bias networks and also adapted to stand-alone clamping. Also, FET devices were successfully employed as clamps, and became even more attractive due to device scaling and the ability to sink ampere-level currents through MOS conduction in a reasonable amount of chip area. Successful power supply clamps have been fabricated from both NMOS and PMOS FETs. In deep submicron CMOS technology, the PMOS FET can be engineered to allow tight layout, high pulsed current density and nondestructive pulsed current flow even beyond the dc punchthrough voltage of the device, and may hold the most promise for present and future power supply clamping in ICs built in these processes.

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Many people at Intel Corporation contributed to the concepts and data herein, extending over several years. The author thanks Sanjay Dabral and Travis Eiles for a large amount of work on the PMOS clamps, and thanks Neal Clark and Krishna Parat for building the cantilever clamps in flash EPROM technology. Other contributors include Andy Volk, Robert Aslett, John Blacker, John Falk, Melik Isbara, Jeff Smith, Glen Wagner and Ed Abratowski. Special thanks go to Tina Cantarero and Wilson Kan for lab work and data presentation.

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