Physical Model for ESD Human Body Model to Transmission Line Pulse

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***Abstract*—A rigorous electrothermal model that describes and correlate the behavior of the ESD devices during TLP and HBM stress conditions for various device types is developed, nearly five decades after well-known Wunsch-Bell and Tasca models.**

Keywords—Electrothermal (EOT), Thermal Runaway (TRA), Transmission-Line Pulse (TLP), Electrostatic Discharge (ESD)

I. Introduction

Joule-heating induced the thermal runaway is the most important failure mechanism of the electrostatic-discharge (ESD) protection device under ESD stress conditions. Human-Body Model (HBM) is the most important qualification item to determine the ESD robustness of a semiconductor device. The transmission-line pulse (TLP) [1] originally developed as a useful tool to analyze the electrothermal behavior of the device under voltage or current stress since it is a simple square pulse vs exponentially decaying HBM pulse. TLP stress data is commonly used to correlate the HBM ESD performance of the device [2] and several prior publications showed both good and poor correlations [3], [4]. The correlation factor (CF) between HBM failure voltage (and its equivalent current) and TLP current is still the empirical formula, which is based on the output resistor (1.5kΩ) of HBM test (Fig. 1) [2]. From the experiment results, the CF is not a constant number [5], [6], and varies with the device layout.

In this paper, a comprehensive electrothermal model is developed expanding upon the well-known models [7]-[12] with additional insights focusing on the fundamental heat transfer physics. After a review of the basics of heat transfer in the following section, decryption of physical model applicable to both HBM and TLP stress conditions as well as their correlation is presented using three basic devices types, viz., snapback, non-snapback and resistive. The enhancement of the electrothermal model vs the traditional models are also described along with comprehensive theory and measurement data.

II. Basics of Thermal Physics

The heat equation commonly used to describe the thermal behavior of the device under the voltage or current stress is

$$\frac{\partial U(x,t)}{\partial t} = \alpha \frac{\partial^2 U(x,t)}{\partial x^2} + H(x,t) \quad (1)$$

where $\alpha=k/\rho C$, k is the thermal conductivity, ρ is the density and C is the specific heat capacity.

This is based on the energy conservation law as illustrated in Fig. 2, where the heat storage rate ($\rho C\partial U(x,t)/\partial t$) is equal to the sum of the heat generation and dissipation/transfer rates ($\rho CH(x,t)-k(\partial U(x,t)/\partial x-\partial U(x+dx,t)/\partial x)$). Most classical models [7]-[11] treated the heat problem for a semiconductor under the voltage or current stress as the semi-infinite problem. If this is the semi-infinite problem, heat only can be conducted from heat source to the region outside it and there is no heat conducted into the heat source, e.g., from the left hand side ($k\partial U(x,t)/\partial x=0$) since it is hotter than other regions and located on the leftmost region. In most ESD stress cases, the region of heat source is much smaller than the region outside it. Moreover, there is no heat generation at the region outside heat source for most devices under the voltage and current stress. So, Eq. (1) can be modified to different heat equations for two different regions, where one heat equation is without the heat dissipation or transfer rate term ($\partial^2 U(x,t)/\partial x^2=0$) and another heat equation without the heat generating rate term ($\rho CH(x,t)$). Incorporated the two heat equations, a general equation for semiconductor device under the ESD or TLP stress is presented in this paper. Based on this new model, the correlation factor, CF, for HBM versus TLP is derived and the detailed physical insight of the CF is also investigated and presented.

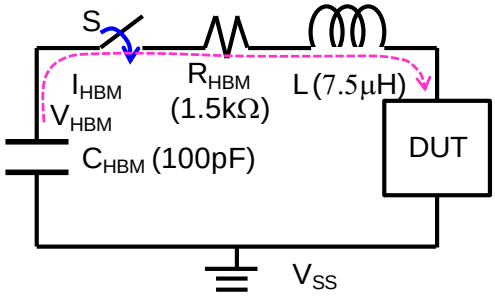

Fig. 1. Simplified equivalent circuit for HBM.

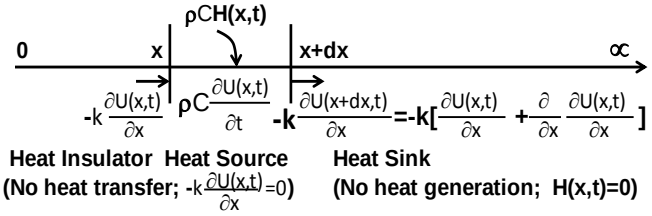

Fig. 2. One dimensional heat conduction through a large plane in a semi-infinite body.

III. Physical Model

A. HBM Discharge Current

Fig. 1 shows the simplified equivalent circuit of a device under the HBM event. Compared to the 1.5kΩ resistor, the device Ron is too small. So, the device I_{HBM} can be approximated to the short circuit HBM current [13].

$$I_{HBM}(t) = \frac{V_{HBM}}{2bL}\left[e^{(-a+b)t} + e^{-(a+b)t}\right] \quad (1)$$

where $a = \frac{R_{HBM}}{2L}$, and $b = \frac{\sqrt{(R_{HBM}+C_{HBM})^2 - 4LC_{HBM}}}{2LC_{HBM}}$.

Using this equation, the calculated current of a typical snapback device, grounded gate nMOS device (GGNMOS), during the 2kV HBM event (Fig. 3) match to the measurement, clearly demonstrating its validity to describe the device discharge behavior. By neglecting the rising transient, the HBM current of the device after 10ns can be simplified to

$$I_{HBM}(t) = \frac{V_{HBM}}{R_{HBM}} e^{-t/(R_{HBM}C_{HBM})} = I_{HBMO} e^{-\mu t} \quad (2)$$

where $I_{HBMO}=V_{HBM}/R_{HBM}$, and $\mu=1/(R_{HBM}\times C_{HBM})$.

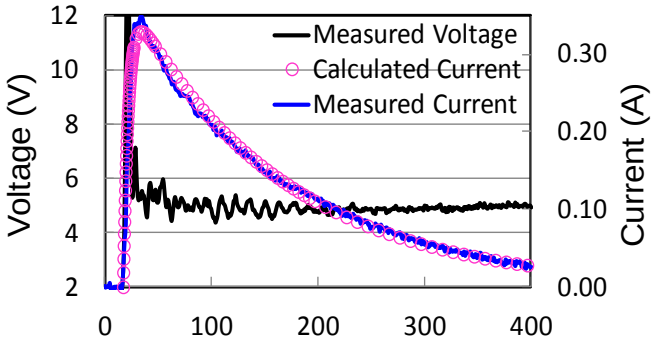

Fig. 3. Measured and calculated 0.5kV HBM voltage and current waveforms of the GGNMOS (Total Width=360um in Table I).

B. Electrothermal Model for HBM and TLP

Fig. 4 schematically illustrates the heat generation and conduction for a device under the HBM event. The heat generation rate can be expressed as $P(t)=V_{SP}\times I_{HBM}(t)$, where V_{sp} is the snapback voltage. Part of the heat is transferred outside the device by the temperature gradient $(-kA\partial U(x,t)/\partial x)$ and the rest of heat is stored in the device to increase its temperature $(\rho CA_H d\partial f(t)/\partial t)$. Based on the law of energy conservation, the electrothermal equation of the device under the HBM event is

$$\rho C A_H d\frac{\partial f(t)}{\partial t} = P(t) + kA_H\frac{\partial U(0,t)}{\partial x} \quad (3)$$

where $A_H d$ is the device turn-on volume [14] and assumed as equal to $Adexp(-\zeta t)$ in response to the exponential decay I_{HBM} from EMMI result in [15], A_H is the device turn-on area in the yz plane, and d is the maximum distance in the normal direction of yz plane (x-axis) that the current flows through.

Without heat generation, the heat equation at the region outside the device from Eq. (1) is

$$\alpha\frac{\partial^2 U(x,t)}{\partial x^2} = \frac{\partial U(x,t)}{\partial t} \quad (4)$$

subject to $U(0,t)=f(t)$, $U(x\to\infty,t)=0$, $U(x,0)=0$

Taking Laplace transformation of Eq. (4), the general solution [16] for the heat equation with semi-infinite region outside the device is

$$U(x,S) = F(S)e^{-x\sqrt{S/\alpha}} \quad (5)$$

Taking the derivative of T(x,S) at x=0,

$$\frac{\partial U(0,S)}{\partial x} = -\sqrt{\frac{S}{\alpha}}F(S) \quad (6)$$

Taking Laplace transformation of Eq. (3) and substituting Eq. (2) and Eq. (6) into it yields

$$F(S) = \frac{P_{HBM}}{\rho CAd\left(S+\mu-\zeta\right)\left(S+\sqrt{\frac{k}{\rho Cd^2}S}\right)} = \frac{P_{HBM}}{\rho CAd(S+\beta)(S+\sqrt{\gamma S})} \quad (7)$$

where $P_{HBM}=V_{SP}V_{HBM}/R_{HBM}$, $\gamma = k/(\rho Cd^2)$ and $\beta=\mu-\zeta$.

This equation also can be obtained by the thermal ohm's law [17], [18]. The thermal impedance for a device under the voltage or current stress is [19]

$$Z(S) = \frac{1}{\rho CAd(S+\sqrt{\gamma S})} \quad (8)$$

In accordance with [19, the "S" term could be adjusted to allow for properties of metal in the heat source layer. Laplace transform of power generation rate P(s) for the device under the HBM event is $P_{HBM}/(S+\beta)$ from Eq. (2) and Eq. (7).

According to the thermal Ohm's law [17-19], the Laplace transform of temperature for the device under the HBM is

$$F(S) = P(S)Z(S) = \frac{P_{HBM}}{\rho CAd(S+\beta)(S+\sqrt{\gamma S})} \quad (9)$$

This equation is identical to Eq. (7).

Applying the inverse Laplace transform $\left(L^{-1}\left(\frac{1}{S+\sqrt{\gamma S}}\right) = e^{\gamma t}\,\mathrm{erfc}(\sqrt{\gamma t})\right)$ [19], [20], the temperature of the semiconductor device under the HBM stress is

$$f(t) = \frac{P_{HBM}}{\rho CAd}\int_0^t e^{-\beta(t-\tau)}e^{\gamma\tau}\,\mathrm{erfc}(\sqrt{\gamma\tau})d\tau$$

$$= \frac{P_{HBM}}{\rho CAd(\gamma+\beta)}\left[\mathrm{erfc}(\sqrt{\gamma\tau})e^{(\beta+\gamma)\tau}e^{-\beta t}\Big|_0^t + \int_0^t e^{-\beta t}e^{(\gamma+\beta)\tau}d(\mathrm{erf}(\sqrt{\gamma\tau}))\right]$$

$$= \frac{P_{HBM}}{\rho CAd(\gamma+\beta)}\left[\mathrm{erfc}(\sqrt{\gamma t})\,e^{\gamma t} - e^{-\beta t} + \frac{2}{\sqrt{\pi}}\int_0^t e^{-\beta t}e^{\beta\tau}d\sqrt{\gamma\tau}\right]$$

Let $\tau=\xi^2$, $\xi=\sqrt{\tau}$

$$= \frac{P_{HBM}}{\rho CAd(\gamma+\beta)}\left\{\mathrm{erfc}(\sqrt{\gamma t})\,e^{\gamma t} - e^{-\beta t} + 2e^{-\beta t}\sqrt{\frac{\gamma}{\pi\beta}}\int_0^{\sqrt{\beta t}} e^{(\sqrt{\beta}\xi)^2}\,d\sqrt{\beta}\xi\right\}$$

$$= \frac{P_{HBM}}{\rho CAd(\gamma+\beta)}\left[e^{\gamma t}\,\mathrm{erfc}(\sqrt{\gamma t}) - e^{-\beta t} + \sqrt{\frac{\gamma}{\beta}}e^{-\beta t}\mathrm{erf}\,(\sqrt{\beta t})\right]$$

$$\approx \frac{V_{HBM}V_{SP}}{\rho CAd(\gamma+\beta)R_{HBM}}\left[\mathrm{erfc}(\sqrt{\gamma t})e^{\gamma t} - e^{-\beta t} + 2\sqrt{\frac{\gamma}{\pi\beta}}e^{-\beta t}\sqrt{\beta t}\right]$$

$$\approx \frac{V_{HBM}V_{SP}}{\rho CAd(\gamma+\beta)R_{HBM}}\left[\mathrm{erfc}(\sqrt{\gamma t})e^{\gamma t} + (2\sqrt{\frac{\gamma t}{\pi}} - 1)e^{-\beta t}\right] \quad (10)$$

Assuming $\mu=0$, Eq. (2) also can be used to depict the current of the device during the TLP stress since it is a square current pulse (Fig. 5). Substituting $\beta=0$ into Eq. (10) and using I_{TLP} instead of I_{HBMO} (V_{HBM}/R_{HBM}), the temperature of the device during the TLP stress is obtained as

$$f(t) = \frac{I_{TLP}V_{SP}}{\rho CAd\gamma}\left[\mathrm{erfc}(\sqrt{\gamma t})\,e^{\gamma t} + (2\sqrt{\frac{\gamma t}{\pi}} - 1)\right] \quad (11)$$

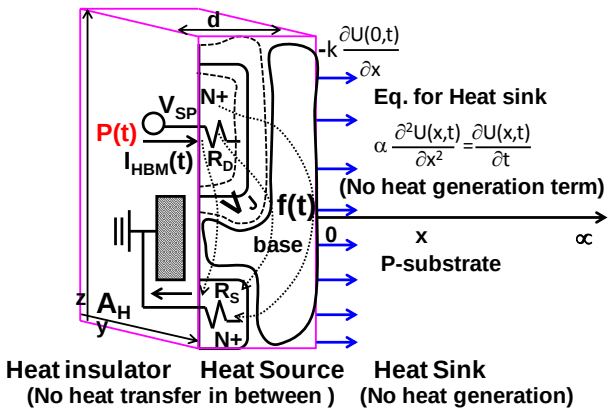

Fig. 4. Schematic depiction of heat generation and conduction for a GGNMOS device under a HBM stress event.

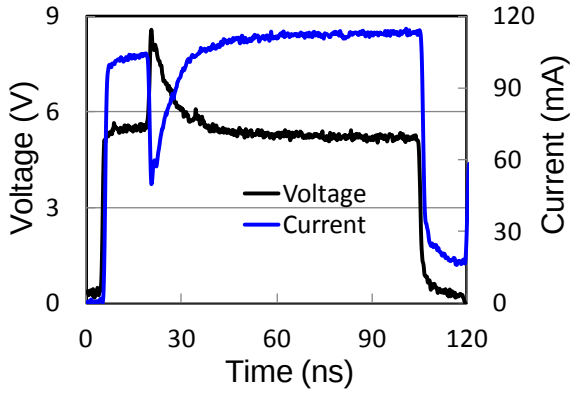

Fig. 5. Voltage and current waveforms of the GGNMOS (total width 360um in Table I) under a 0.12A TLP.

C. Electrothermal Model for Correlation Factor

The main failure mechanism for device during the TLP or HBM stress is the thermal runaway caused when the device temperature reaches the melting point of silicon. Based on this failure criterion (Eq. (10=Eq. (11)), the CF is

$$CF = \frac{V_{HBM}}{I_{t2}} = \frac{R_{HBM}(\gamma+\beta)\left[\operatorname{erf c}(\sqrt{\gamma t_T})e^{\gamma t_T}+2\sqrt{\frac{\gamma t_T}{\pi}}-1\right]}{\gamma\left[\operatorname{erfc}(\sqrt{\gamma t_H})e^{\gamma t_H}+\left(2\sqrt{\frac{\gamma t_H}{\pi}}-1\right)e^{-\beta t_H}\right]} \quad (12)$$

where t_T and t_H are the times to failures of the device for the TLP stress and HBM stress with t_T=100ns for a 100ns TLP.

IV. Model Validation and Discussions

The devices used for validating the newly developed model are: (a) N+ Nickel silicide poly resistor, (b) 2.5V MOFET's and (c) N+/PW diodes, which are all fabricated on a mature high volume CMOS technology process. Commercial calibrated HBM and TLP testers are used for the experimental evaluations. The TLP tester used a standard 100ns pulse width.

A. W-B Model and New Model Validation

Fig. 6 shows the voltage and current waveforms in silicided N+ poly resistor under a 100ns TLP stress event. Between ~-24ns to 0ns, the pulse travels through the cable from the TLP system to the device under test. When the pulse transient arrives at the resistor (~0ns), the voltage increases from 4.2V to 6.5V due to the impedance mismatch. After this transient, the voltage and current change with time, attributed to the Joule-heating induced the resistance change. Fig. 7 shows the time varying resistance (R=V/I) and power (P=VI) based on the measured waveforms in Fig. 6. The resistance increases from 170Ω to 300Ω and saturates to 300Ω between 48ns and 55ns, and then decreases with time. The power only slightly decreases with time (0.22W-0.19W) and therefore can be assumed as a constant for whole stress period. So, this TLP measurement can be used to verify the electrothermal behavior of the resistor against Wunsch-Bell model [7] and the new model since both models assume constant power.

Most resistors fabricated on CMOS technology have positive temperature coefficient below the critical temperature. With this characteristic, the temperature of a resistor under the TLP is $T(t)=(R(t)/R_o-1)/\beta$ (13)

From the measured resistance in Fig. 7 and Eq. (13), the temperature of silicided N+ poly resistor under the TLP stress is shown in Fig. 8. The temperature increases with time from the room temperature until ~1000°C, and then saturates at 1000°C after 48ns. The temperature saturation is attributed to loss of silicide ($NiSi_2$) adhesion and it agglomerates into the polysilicon as the temperature increases to 1000°C [21], as confirmed by the TEM image, Fig. 9. This gives a direct physical evidence that the temperature extracted from the measured voltage and current waveforms accurately depict the temperature of the resistor under the TLP stress.

Fig. 8 also confirms that the calculated temperature based on the new model (Eq. (11)) match to the extracted temperature from measurement data below the $NiSi_2$ agglomeration temperature. However, the calculated temperature based on the W-B model ($f(t) = \frac{P}{Ad}\sqrt{\frac{t}{\pi\rho kC}}$) [7] only fits the extracted temperature from measurement data within first 15ns and starts to deviate from the evaluated curve. This demonstrates that new model can depict the thermal behavior of the resistor better than the Wunsch-Bell model, improving the predictability by 3x. Moreover, the similar result also can be seen in Fig. 11 for the resistor under the stress below the thermal runaway (Fig. 10). The calculated temperature based on the new model (Eq. (11)) match to the evaluated temperature within whole stress period, while the Wunsch-Bell model only fits the evaluated temperature within 20ns, again achieving 3x accuracy in the model predictability.

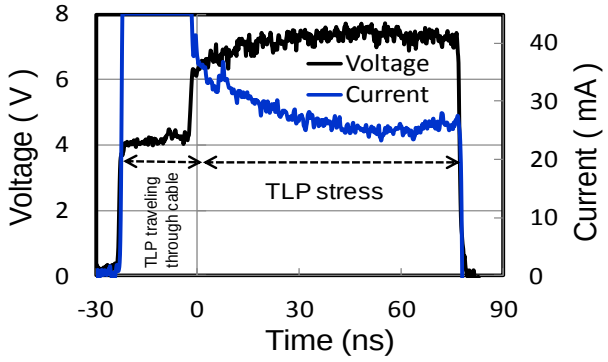

Fig. 6. Voltage and current waveforms of the silicide N+ poly resistor under 100ns TLP pulse for the stress level that can lead to the thermal runaway.

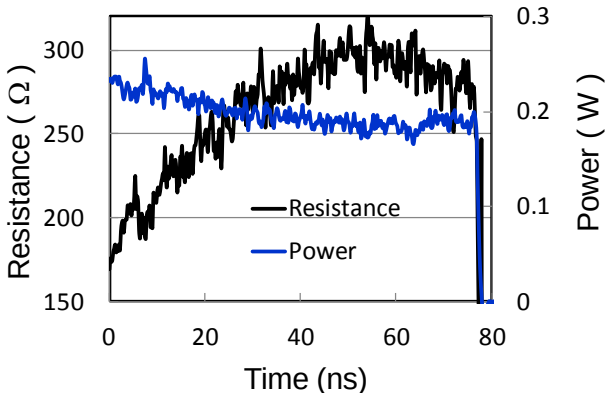

Fig. 7. Measured resistance and power from the waveforms of the silicide N+ poly resistor under 100ns TLP in Fig. 6.

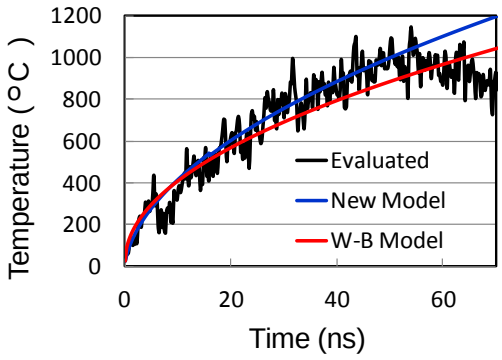

Fig. 8. Extracted temperature based on measured resistance in Fig. 7 and Eq. (13), and calculated temperatures based on Eq. (11), and Wunsch-Bell (W-B) model for silicide N+ poly resistor under the 100ns TLP in Fig. 6.

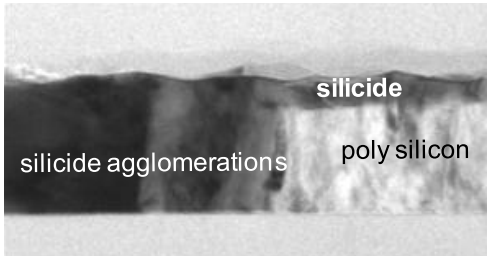

Fig. 9. TEM cross-section of silicide N+ poly resistor after 100ns TLP pulse stress event shown in Fig. 6., showing silicide migration from the top film through and mixes with the poly silicon.

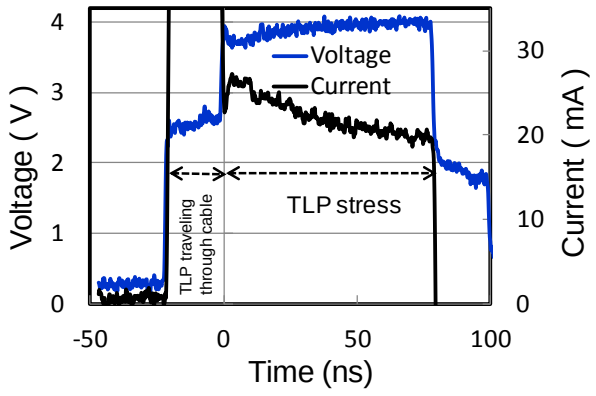

Fig. 10. 100ns TLP stress voltage and current waveforms on the silicide N+ poly resistor at a stress level below the thermal runaway condition.

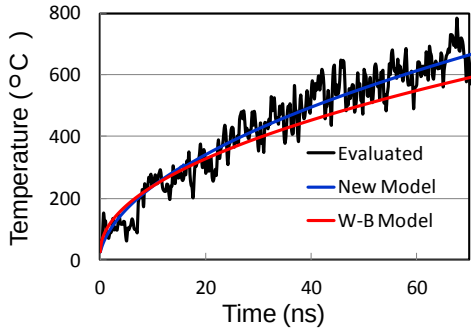

Fig. 11. Extracted temperature based on Fig. 10 and Eq. (13), and calculated temperatures based on Eq. (11), and Wunsch-Bell (W-B) model for silicide N+ poly resistor under 100ns TLP in Fig. 10.

B. CF Model Validation by N/PMOS

The TLP generated power in GGNMOS is a constant since the voltage and current are constants within the snapback region (Fig. 5). As such, the temperature of the GGNMOS under the TLP stress event increases with time according to Eq. (11) (Fig. 12). In contrast, the temperature of GGNMOS under the HBM event first increases with time and remains at the highest temperature for a period (~200ns-300ns), and then decreases with time based on Eq. (10). This demonstrates that the time to induce the thermal runaway to damage the device occurred much after the current peak (~10ns in Fig. 3), at which I_{HBM} decreases with a time constant (μ).

From Eq. (11), the temperature of device under the TLP stress is function of the device density ρ, specific heat capacity C, TLP current I_{TLP}, snapback voltage V_{SP}, stress time t, drawing area A, maximum current distance in x-axis d, and γ which is equal to $k/(\rho Cd^2)$,where k is the thermal conductivity. So, the only unknown parameter in Eq. (11) is "d". For a device under the I_{t2} stress event, the damage is the thermal runaway caused by the Joule-heating induced the temperature of the device higher than the silicon melting point (1414°C). Through the interactive method, the d can be obtained once the temperature of the device is equal to 1414°C at 100ns by substituting the I_{t2}, V_{t2}, ρ, C, k, A, and γ into Eq. (11). As the d is obtained, the only one unknown parameter in Eq. (10) is " β". Based on similar methodology, the β also can be got when the maximum temperature of the device during the HBM stress is equal to 1414°C by substituting the I_{t2}, V_{t2}, ρ, C, γ, A, and β into Eq. (10).

The high current IV characteristics of the devices in Table I under the 100ns TLP stresses are shown in Fig. 13 and Fig. 14. The It2, V_{sp} and CF (V_{HBM}/It2) of the devices extracted from Fig. 13 and Fig. 14 and HBM test result are shown in Table I. It can be seen that the CF is not a constant, which varies with the device dimension and the range is from 1.25k to 1.73k. Except the β, all parameters in Eq. (10) are unchanged with the device structure. The β is the decay time difference ($\beta=\mu-\zeta$) between the I_{HBM} and device turn-on volume. Since the μ is a constant ($1/(R_{HBM}\times C_{HBM})=1/150$ns) from Eq. (2), the parameter that is inducing the CF variation with the device structure should be the ζ. Based on Eq. (10), V_{sp}, V_{HBM} and silicon melting point, the time varying temperature, β, ζ, and CF for the device under the HBM event can be calculated and shown in Fig. 12 and in Table I. It can be seen that the calculated CF's

(CF1) are all the same as the measured CF's. This confirms that the CF varied with the total width (TW) is caused by the ζ. From Table I, the ζ increases as the device TW decreases. This is attributed to the turn-on condition of bipolar $I_{sub} \times R_{sub} \geq 0.7V$, which R_{sub} depends on the position of device (see A or B in Fig. 8) and device TW. As the I_{sub} follows the I_{HBM} to fall, it leads to the device turning off gradually once that regions cannot satisfy the turn-on criterion. With the smaller R_{sub} and I_{sub}, the turn-on area of the smaller TW device (Fig 15) shuts off with the faster speed (ζ) as shown in Fig. 16, resulting in the higher stress current density to lead to smaller HBM performance as shown in Table I. It can be seen that the device HBM performance is not proportional to the device TW, while the device It2 is nearly proportional to the device TW since TLP is a constant stress, which does not lead to the device turn-on area varying with time.

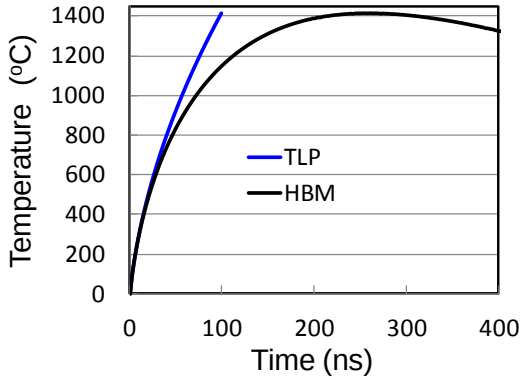

Fig. 12. Calculated temperatures of GGNMOS (total width 360um in Table I under the 2.9A and 5.5kV HBM events.

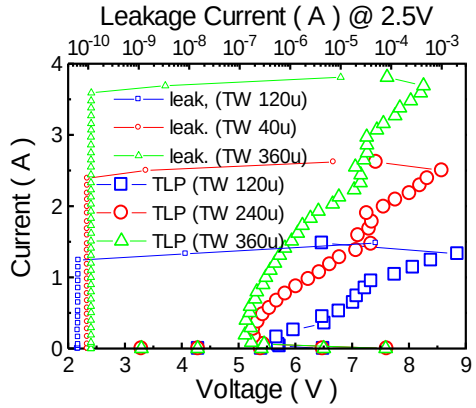

Fig. 13. TLP IV characteristics of GGNMOS devices in Table I.

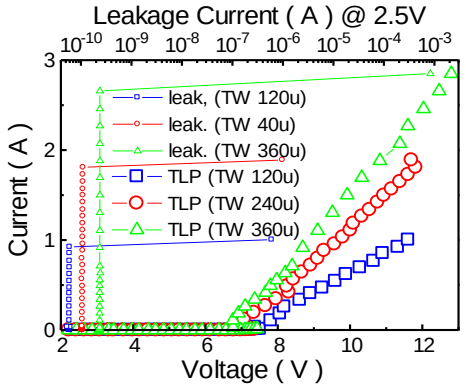

Fig. 14. TLP IV characteristics of GGPMOS devices in Table I.

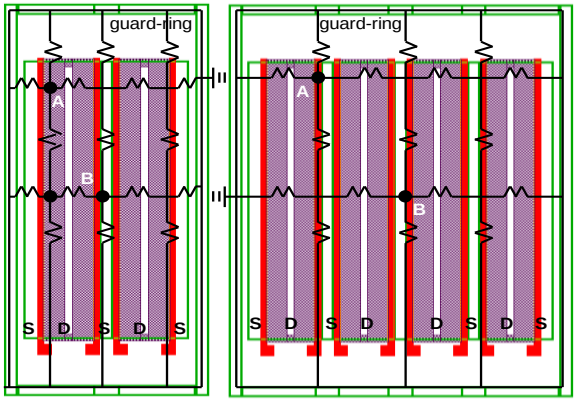

Fig. 15. Top view and substrate resistors for different positions of GGMOS devices (total widths 120um and 240um).

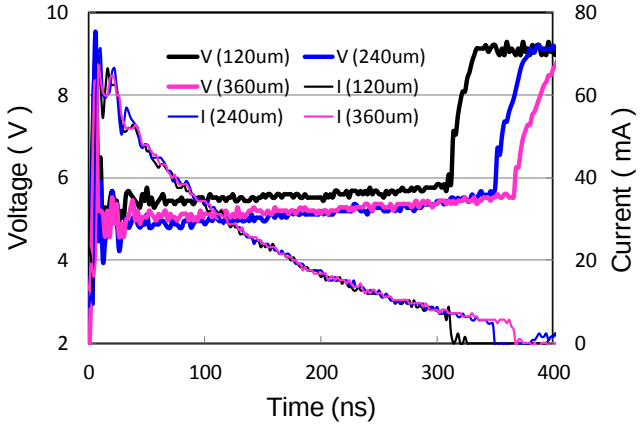

Fig. 16. Voltage and current waveforms on various GGNMOS devices under 100V HBM zapping events.

Table I: Measured CF (V_{HBM}/It2) and calculated CF1 (Eq. 12) for 2.5V GGNMOS/GGPMOS with total width (TW)

MOS	TW	It2	V_{HBM}	CF	V_{t2}	ζ	β	CF1
NMOS	120um	1.2A	1.5kV	1.25k	8.39V	0.79μ	0.21μ	1.249k
NMOS	240um	2.39A	3.75kV	1.57k	8.32V	0.68μ	0.32μ	1.568k
NMOS	360um	3.59A	5.75kV	1.6k	8.2V	0.66μ	0.34μ	1.601k
PMOS	120um	-0.9A	-1.3kV	1.4k	-11.3V	0.72μ	0.28μ	1.446k
PMOS	240um	-1.8A	-3.0kV	1.67k	-11.8V	0.64μ	0.36μ	1.668k
PMOS	360um	-2.6A	-4.5kV	1.73k	-12.5V	0.61μ	0.39μ	1.729k

Note: μ is the decay time constant of I_{HBM}, ξ is the decay time constant for device turn-on volume in response to I_{HBM}, and β is the decay time difference (β=μ-ζ) between the I_{HBM} and device turn-on volumn.

C. CF Model Validation by Diode

Table II shows the layout split, V_{t2}, It2, V_{HBM} and CF of the N+/PW diodes for the TLP test results (Fig. 17 and Fig. 18) and HBM test result. It can be seen that the measured CF's for all diodes in this experiment are almost the same (~1.85k) and is very insensitive to the diode layout.

For a diode under the TLP event, the generated power is a constant since the voltage should be constant in response to a constant current stress. With a constant power, the temperature of the diode under the TLP stress event increases with time

according to Eq. (11) (Fig. 20). Although the falling part of the HBM IV curve of a diode can match its TLP IV curve [22], the IV curves in Fig. 17 or Fig. 18 cannot be transferred to the time domain to depict the transient behavior of the diode under the HBM event. It has been illustrated that the voltage of the diode after the peak voltage of the HBM event falls with another decay time (μ_v) to a constant voltage in response to the exponential decay HBM current [22] and can be assumed as $V_{t2}(1+\exp(-\mu_v t))$. So, the power of diode is $V_{HBM}V_{t2}[\exp(-\mu t)+\exp(-(\mu+\mu_v)t)]/R_{HBM}$ from Eq. (2) and the temperature equation for N/PMOS (Eq. (10)) can be modified as the equation for diode during the HBM event:

$$f(t) = \frac{V_{HBM}V_{t2}}{\rho C A d(\gamma+\mu)R_{HBM}}\left[\mathrm{erfc}(\sqrt{\gamma t})e^{\gamma t} + \left(2\sqrt{\frac{\gamma t}{\pi}} - 1\right)e^{-\mu t}\right] + \frac{V_{HBM}V_{t2}}{\rho C A d(\gamma+\mu+\mu_v)R_{HBM}}\left[\mathrm{erfc}(\sqrt{\gamma t})e^{\gamma t} + (2\sqrt{\frac{\gamma t}{\pi}} - 1)e^{-(\mu+\mu_v)t}\right] = T1+T2 \quad (14)$$

With the similar equation, the temperature of diode under the HBM event increases with time first until reaching the maximum temperature, and then decreases with time as shown Fig. 19. It can be noted that the highest temperature caused by the decay time μ (150ns) is nearly at 100ns. Because of one decay time constant ($\mu+\mu_v$) longer than 150ns, the highest temperature of the diode occurs within 100ns, which is between the maximum temperatures caused by the two time constants. Based on Eq. (14) and Eq. (11), the calculated CF for the diode in Fig. 19 is 1.86k. It is very close to the measured CF 1.85k in Table II but different from the HBM output resistance 1.5k. This is caused by that CF is not only function of HBM output resistance and time to failure but also function of the thermal decay times β (μ-ζ) in Eq. (10) or μ and $\mu+\mu_v$ in Eq. (14).

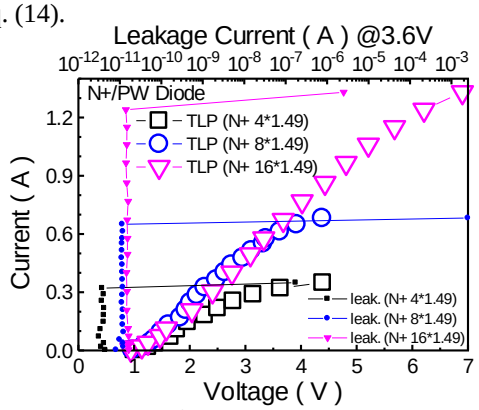

Fig. 17. TLP IV characteristics of N+/PW diodes with varying cathode width.

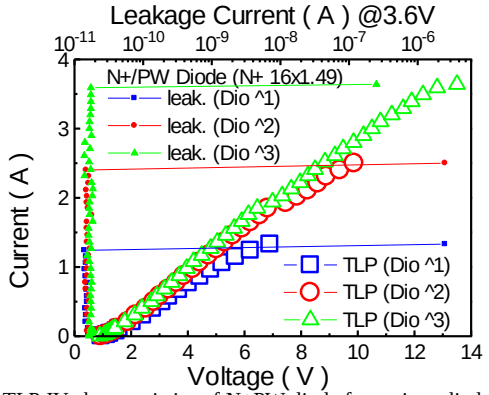

Fig. 18. TLP IV characteristics of N+PW diode for various diodes in Table 1.

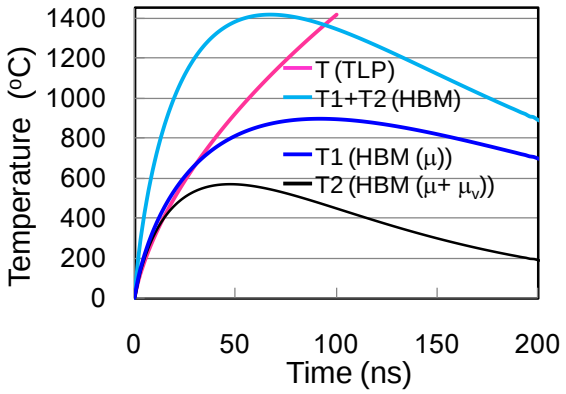

Fig. 19. Calculated temperatures of the N+/PW diode (area 4×1.49um^2 in Table II) under the 0.35A TLP and 0.65kV HBM events.

Table II: Measured CF (V_{HBM}/It2) for N+/PW diodes

N+ area(um^2)	Diode no.	V_{t2}	It2	V_{HBM}	CF
4×1.49	1	3.63V	0.35A	0.65kV	1.85k
8×1.49	1	3.92V	0.65A	1.2kV	1.84k
16×1.49	1	6.21V	1.24A	2.3kV	1.85k
16×1.49	2	9.37V	2.4A	4.5kV	1.87k
16×1.49	3	11.9V	3.59A	6.8kV	1.89k

V. Conclusions

The electrothermal behaviors of ESD protection devices have been extensively studied and a novel physical model which is far better than the classic Wunsch-Bell model developed 50 years ago is described. Using one equation, the electrothermal behavior of the traditional ESD devices such as a resistor, diode and snapback device matching to HBM and TLP experimental data can be predicted. The TLP event is the special case of the HBM event, where the RC decay time μ is zero. The model is also able to explain physical mechanism of device response under HBM or TLP and the correlation factor (CF) between HBM and TLP stress results for various ESD protection devices.

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