Versatile Models and Expanded Application of the IEC 61000-4-2 Test

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Abstract - An all-purpose circuit model and associated shorting current waveform expression for the IEC 61000-4-2 pulse is presented. Criteria include agreement with existing IEC guidance plus zero field derivative at t=0, for accurate radiation modeling. Also, a capacitive coupling tool for IEC pulsers is used to simulate platform I/O port hazards.

I. Introduction

The IEC 61000-4-2 system ESD test is standardized through current waveform measurements into a 2-ohm target [1], and the standard can be met simply by satisfying the rise time, peak current, and current at 30 and 60 nsec to within tolerance, and only for that 2-ohm load, nearly a short circuit. Accordingly, many pulser guns are deemed adequate for system testing, yet produce varying test results. These problems are well known, not easily solved, and a major source of discussion in the industry. One aspect of that discussion has been to describe the near-short circuit waveform analytically, possibly with an associated circuit model. IEC pulses into chassis metal, per the standard, are likely to be similar, and these are useful for modelling. However, among the many treatments, the concise circuit model that also corresponds to a compact analytic expression is the exception rather than the rule. More common is the analytic expression in the IEC standard itself [1], from the Heidler equation from work in lightning, for which there is no simple corresponding circuit model. In this work, we examine a full set of criteria for an IEC 61000-4-2 model, and see if a circuit model, corresponding analytic form for the short circuit, and other criteria can be formulated. Much existing work is useful and will be cited; however, the modeling criteria have been influenced and expanded due to related ESD hazards and effects that have recently been identified. These new findings will be described in some depth, and their influence on the IEC models noted.

A proper set of criteria for an all-purpose model of the IEC 61000-4-2 pulse should start with a (concise) analytic formula and circuit model in tandem, satisfying the IEC waveform specs [1] and approximating the analytic waveform in [1]. The full list of IEC model criteria for this work is:

1. Exact agreement of analytic form and circuit model for short circuit (or 2-ohm target) IEC waveform. Concise expression of each (e.g., lumped circuit elements) is highly desirable.
2. Agreement with IEC current waveform specs [1] but with close tolerance. Good agreement with the Heidler waveform as in [1], but with improvements.
3. Circuit model correctly accepts higher-Z load conditions such as series capacitance, and results agree with measured waveforms.
4. Third derivative of current is zero at t=0 ($i'''(0)=0$) so that nearby noise-inducing dE/dt and dH/dt will start up from zero, as expected from physics.

Criteria (3) and (4) are relatively unusual, although (3) was treated in some depth at the 2014 EOS/ESD Symposium [2], showing the importance of platform and board size (from cell phones and smaller to large boxes), plus the horizontal coupling plane (HCP) interaction. Criterion (3) also applies to a newly-reported failure mechanism for flash drives with unshielded “A”-type USB connectors, where the stress is well expressed by a series capacitance-coupled IEC pulse. That stress can be approximated by a test using a simplified ground return and an IEC gun probe tool having built-in series capacitance, in an adjusted form of the Human Metal Model (HMM) test [3]. Finally, Criterion (4) recognizes the importance of the pulse current startup transient in any E- and H-field calculations aimed at finding disturbances on nearby electronics (say on PC board microstrip lines). The author’s work on field

detectors from 2008 [4] began earlier with measurement and calculation of board trace effects caused by nearby IEC zaps to ground, whereby the induced signals depend on field derivatives. Thus we do not want any unphysical impulses or abrupt steps in the calculated signal at t=0. This may not always be a strong concern for IEC current modeling, but it turns out to be straightforward to incorporate the related features into an all-purpose model. In a later section, we will review some of these previously unpublished measurements and calculations of induced current/voltage in microstrip lines from the IEC zap.

II. Analytic Expressions and Circuit Models

We start with two studies that satisfy our first two criteria, (1) and (2), and begin to accommodate (3). We then see how some refinements can further treat criteria (3) and (4).

A study from Mertens, et al. in 2012 [5] provided models for Tazzoli [2] and even began the studies of a series capacitor load. The model of [5] for the "nominal" waveform into a shorting target has elements as in Figure 1, with the series cap to be inserted later. The network is solved for an equivalent admittance $Y_T=Y_A+Y_B$ as in Figure 2 through a conventional Y-Δ transformation that is made simpler by the common node to the step generator at the bottom. The result is admittance

$$Y_T(s)=\frac{Z_3+Z_2}{Z_1Z_2+Z_2Z_3+Z_1Z_3} \quad . (1)$$

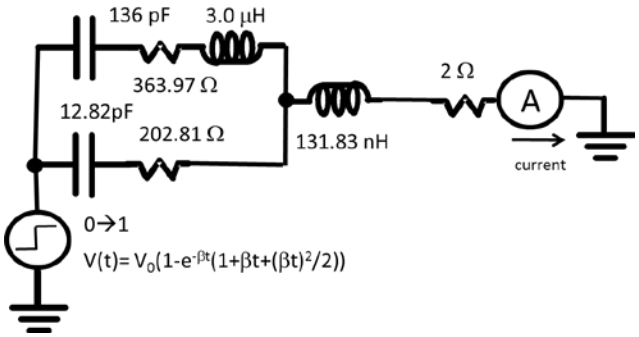


Figure 1: Circuit model for "nominal" waveform, from [5]. Here we use a "soft" step function, β=15 GHz.

The current transfer function I(s) thus has four poles and two zeroes (s is complex frequency; s=σ+jω). Accordingly, the current starts at zero but with nonzero derivative (i.e., $I(s)\rightarrow 1/s^2$, a linear ramp, as $s\rightarrow\infty$). For i′′′(0)=0 at t=0, as above, we need 3 more poles, but they can be introduced with a "soft" step function for voltage, say with $V(s)=\frac{V_0}{s(1+\alpha s)^3}$

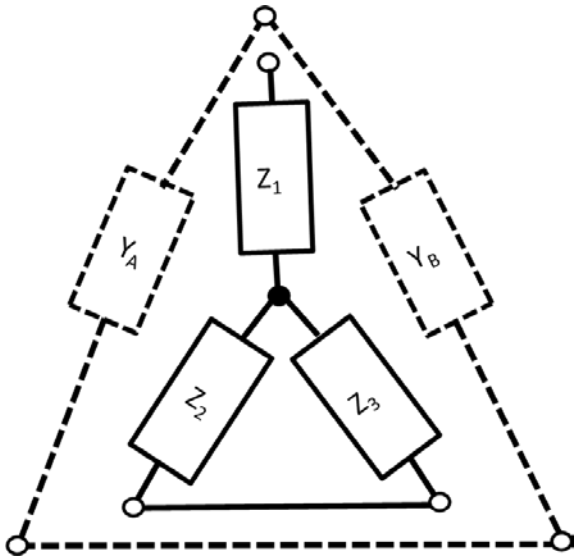


Figure 2: Z_1-Z_2-Z_3 "Y" network of Fig. 1 converts to Y_A-Y_B "delta" network such that admittances add due to the Z_2-Z_3 short.

replacing V_0/s, α a time constant. This corresponds to a step voltage source of the form $V_0(1-e^{-\beta t}(1+\beta t+(\beta t)^2/2))$, $\beta=1/\alpha$. The full s-domain expression can thus become a time domain expression for the current, through the inverse Laplace transform, using Mathematica software. The resulting current is a few percent high even for the soft step function, so no elements were changed. For Fig. 1 with a soft step (β=15 GHz; Elmore delay rise time of 3α=200 psec), the resulting current function is

$$I(s)=\frac{148.82V_0(1+\tau_{z1}s+(\tau_{z2}s)^2)}{(1+\tau_r s)^3(1+\tau_{p1}s+(\tau_{p2}s)^2+(\tau_{p3}s)^3+(\tau_{p4}s)^4)} \quad (2)$$

I(s) will invert to amps if V_0 is in kV, s in GHz and the τ quantities in nsec. The τ quantities are τ_{z1}=6.6402, τ_{z2}=6.057, τ_r=0.0667, τ_{p1}=52.398, τ_{p2}=23.628, τ_{p3}=10.632, τ_{p4}=5.180 nsec. This inverts to the time domain (with t in nanoseconds) to become, for V_0=1kV,

$$i(t)=A(e^{-s_1t}-e^{-s_2t})+B(e^{-s_3t}-e^{-s_4t})+\Delta_{12}e^{-s_1t}+\Delta_{34}e^{-s_3t}+a_1e^{-s_rt}(1+f_1t+(f_2t)^2); \quad (3)$$

A= 4.9194, B=41.0804, Δ_{12}= -0.00298, Δ_{34}= -1.86, a_1=1.86298 amps; s_1=0.02578, s_2=0.09106, s_3=0.6709, s_4=0.8820, s_r=15, f_1=9.494, f_2=5.814 GHz. Note that all real pole frequencies result from the "nominal" lumped element values of [5] as shown in Fig. 1. This is not always the case for IEC-compatible waveforms; other element choices from [5] give complex conjugate poles, and include sine and cosine functions in i(t). Figure 3 compares Eqn. (3) to the Heidler expression in [1], at long and short time scales. The Heidler expression in [1] is as follows, for 1kV:

$$I(t) = \frac{I_1}{k_1} \cdot \frac{\left(\frac{t}{\tau_1}\right)^n}{1+\left(\frac{t}{\tau_1}\right)^n} \cdot \exp\left(\frac{-t}{\tau_2}\right) + \frac{I_2}{k_2} \cdot \frac{\left(\frac{t}{\tau_3}\right)^n}{1+\left(\frac{t}{\tau_3}\right)^n} \cdot \exp\left(\frac{-t}{\tau_4}\right) \quad (4)$$

where

$$k_1 = \exp\left(-\frac{\tau_1}{\tau_2}\left(\frac{n\tau_2}{\tau_1}\right)^{1/n}\right) \qquad k_2 = \exp\left(-\frac{\tau_3}{\tau_4}\left(\frac{n\tau_4}{\tau_3}\right)^{1/n}\right)$$

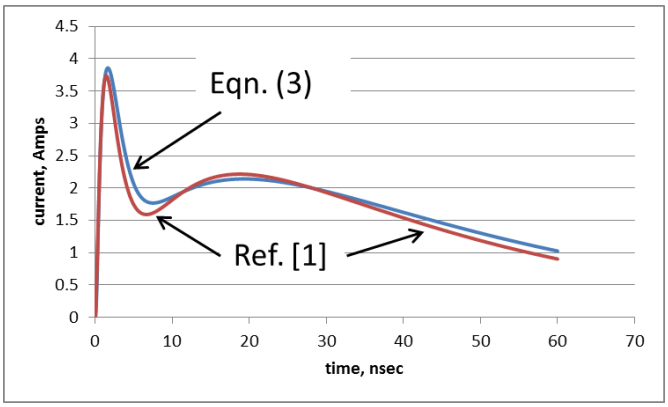
and τ_1=1.1 ns; τ_2=2 ns; τ_3=12 ns; τ_4=37 ns;

I_1=4.15 A (at 1kV); I_2=2.325A (at 1 kV); n=1.8.

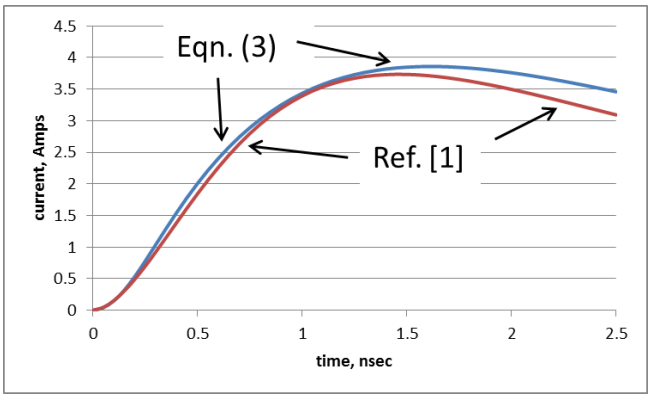
Because n=1.8, the expression (4) has a "soft" startup transient, but i‴(0)>0 at t=0 because n=1.8. For the 3rd derivative of current to vanish, n≥3 is required in the Heidler expression (this was the case in some earlier work [6]). But Eqn. (3) meets Criterion (4) because of the triple pole in Eqn. (2), as now $s^3I(s) \rightarrow 1/s^2$ as $s \rightarrow \infty$, i.e., 3rd derivative of current is a linear ramp starting at 0 for t=0.

A second study from 2012, by Wang, et al. [7], constructed the IEC waveform from two double-pole current expressions, added in parallel for a current function I(s) that again has 4 poles and 2 zeroes. The parallel currents (each of the form $i(t)=Ate^{-\alpha t}$) resulted in a current waveform and comparison to [1] that was very close, and in agreement with all waveform parameters. The authors then solved for the parallel RLC branches giving the double poles; values are shown in Figure 4.

In [7], Wang, et al. added a 1-ohm resistor in the Z_1 (see Fig. 2) branch of the "Y" network, despite the 2-ohm resistor specified in [1]. Either way, the extra branch splits the double poles, however slightly. But the poles will split even more when we consider nonzero impedance loads like added capacitance in the Z_1 branch, in a later section of this work. We use 2 ohms in this work because of the 2 ohms in the standard target of [1], and also use the "soft" step function at all times. When we solve the network of Fig. 4, with 2-ohm load and the soft step function, we get agreement with [1], resembling Figs. 2-3, and close agreement with all IEC waveform specs. Models of IEC 61000-4-2 for the shorting load as in Figs. 1 and 4 are very similar and will both be used as prototypical IEC circuit models in this work.



(a)



(b)

Figure 3: Short circuit IEC waveforms compared at (a) long and (b) short time scales.

III. Relevance of IEC with Adjusted Load Conditions

Series capacitance is treated in Refs. [2, 5] mostly in the context of the HCP element, plus the additional series capacitance of a small board or platform. These are important considerations for IEC 61000-4-2 testing on more and more smartphones, devices for internet of things (IoT), and such, but the series capacitance involved in some direct ESD threats to I/O ports is also important.

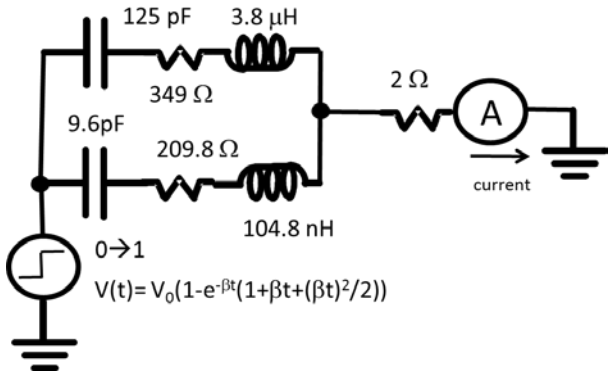


Figure 4: Model from [7], inspired by fitting double-pole functions ($i(t)=Ate^{-\alpha t}$) to the IEC waveform.

A. Flash Drives and SD Cards

Consider the USB flash memory drive as pictured in Figure 5. In this low-cost embodiment of a Type A USB2 connector, there is no box-like metal shield around the 4 pins. The shield virtually guarantees first contact to the platform's metal chassis, as would also be the case for a standard USB2 cable with Type A connectors. Data pin damage could only happen through rather weak induced currents [8]. But with no shield, the four USB2 pins are threatened. The USB2 standard correctly has the interior I/O pins being recessed as shown, meaning they are less likely to contact first than the outer Vcc/Vss pins. So the importance of tolerating direct zaps to USB2 Vcc/Vss (and under powerup conditions) is foremost, followed by data I/O pin tolerance.

Figure 5: Flash memory drive with Type A USB2 connector having no metal shield.

The anticipated stress to USB2 pins (of a platform receptacle as well as to the flash drive's) would be capacitive coupling through the dielectric body of the memory, to the charged human holding it, in an uncontrolled environment. The equivalent capacitance may be only picofarads, and the human may not discharge completely, but clearly there is a final dipole established, with opposing charge under the thumb, literally, of the human holding the so-called thumb drive. Current flow can be approximated by the IEC pulse into a capacitive load, where the up-front current spike is largely preserved and the follow-on decaying pulse is severely muted [2,5]. A similar event can be expected with SD cards as they are plugged in, as there is no shield-shield discharge built into the standard construction. Of course, an open USB or other cable may have isolated I/O lines that have become tribocharged (say, due to flexing), and so certain weak transmission-line pulse (TLP) events could happen to I/O lines after power and ground lines are connected.

B. Hardware Tool to Simulate Capacitive Coupling

Testing platform port I/O pins for this kind of ESD hazard can be done using the IEC pulser in accordance with conditions suggested by the HMM test [3], but how do we easily capture the series capacitance and apply a realistic stress to the pins? Figure 6 shows an IEC pulser gun probe that can be used to build the desired series capacitance into the pulser itself. A dielectric sheath and secondary probe are built onto an interior probe with the usual shaft diameter. With this means to capture capacitive coupling, no additional fixturing is needed for the broken-out I/O pins, and the ground strap can be returned to the chassis (as with HMM [3]) for simplicity.

The kind of pulse we get into the 2-ohm target with the capacitive coupling tool is shown in Figure 7b in red, for 1kV. The attenuated long tail is reproduced almost exactly using the Fig.7a (Fig. 4 with series cap) model for this probe, measured as 25 pF at 1 MHz. The result is virtually the same were we to start with Fig. 1 plus series cap, and it also follows low series cap results in [2]. However, the simulated I_{peak} is too high. But when the bypass capacitance of the gun body itself and the coupling tool is added as a 15 pF lumped element as in Figure 8a, the simulated result in Fig. 8b agrees remarkably well with the measurement. This bypass capacitance affects the waveform only for the elevated impedance load, such as the 25 pF, because for a near short (Figs. 1 and 4) it has negligible influence.

The simulations for Figs. 7b and 8b were again done with Mathematica (as for Eqs. 2-3 earlier), although Spice simulations give the same curves. We now present the s-domain and time domain solutions for the current, per kV of step voltage.

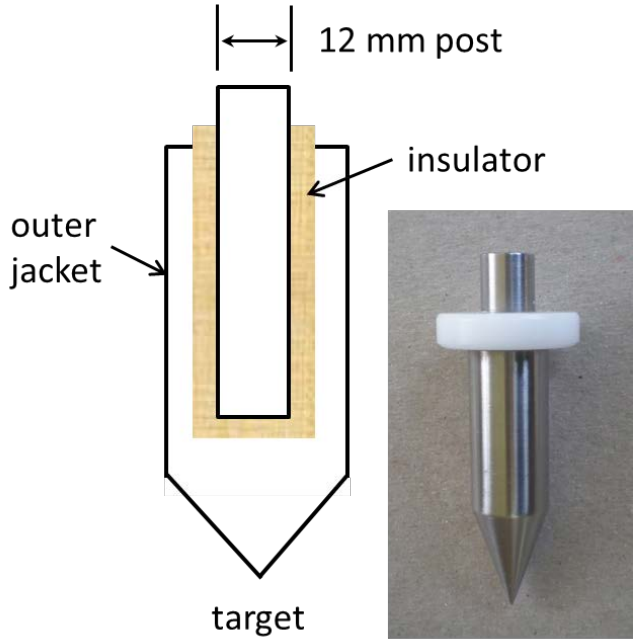
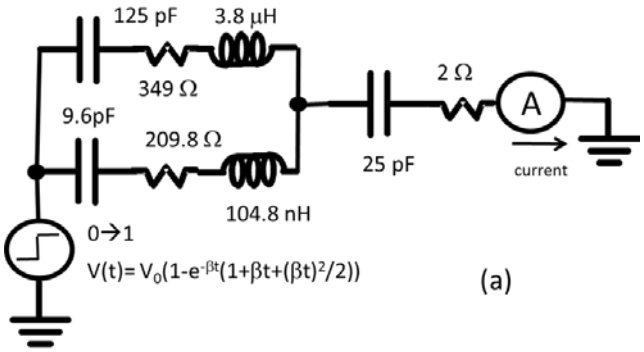


Figure 6: Schematic drawing, and inset photo, of capacitive coupling tool for an IEC pulser. Metal probes are separated by Delrin® dielectric, and series capacitance of 25 pF is measured.



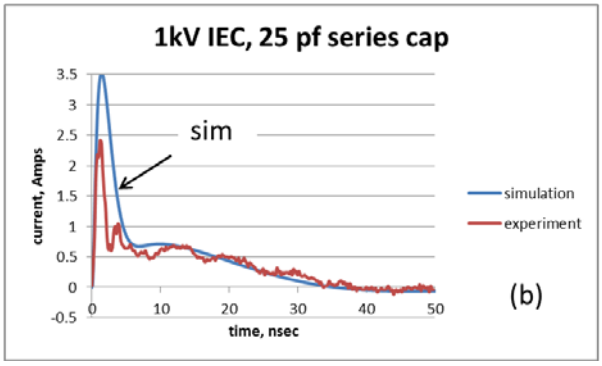
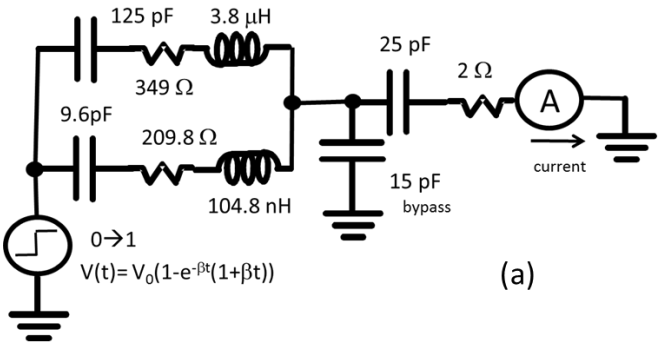


Figure 7: (a) Circuit as in [7], and Fig. 4, plus 25 pF for coupling tool as in Fig. 6. β=15 GHz. (b) Current into 2-ohm target for 25 pF series cap as in (a), but simulated peak current for 1 kV comes out much higher than the measured 2.42 amps.



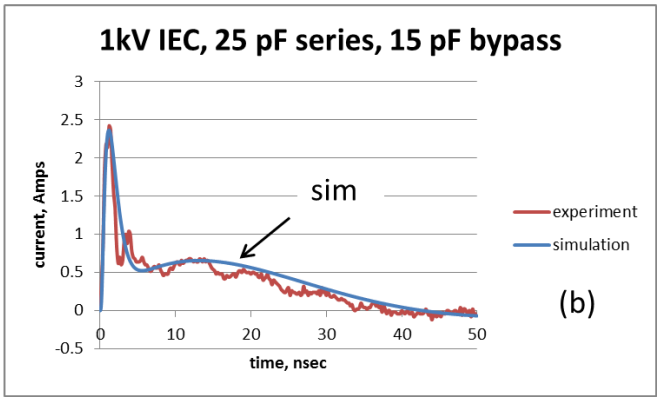


Figure 8: (a) Circuit as in Fig. 7a plus 15 pF bypass capacitance; β=11.1111GHz. (b) Current into 2-ohm target for coupling tool, same as Figs. 6-7, but now with series and bypass cap simulated as in Fig. 8a. Measured waveform is now closely matched.

$$I(s) = \frac{19.27V_0(1+\tau_{z1}s+(\tau_{z2}s)^2)}{(1+\tau_r s)^2 P_5(s)}\ , \text{where}$$

$$P_5(s) = 1+\tau_{p1}s+(\tau_{p2}s)^2+(\tau_{p3}s)^3+(\tau_{p4}s)^4+(\tau_{p5}s)^5 .$$

(5)

As before, I(s) will invert to amps if V_0 is in kV, s in GHz and the τ quantities in nsec. The τ quantities are τ_{z1}=4.98009, τ_{z2}=5.9002, τ_r=0.09, τ_{p1}=14.337, τ_{p2}=12.505, τ_{p3}=6.1482, τ_{p4}=3.2347 and τ_{p5}=1.55048 nsec. This inverts to the time domain (with t in nanoseconds) to become, for V_0=1kV,

$$i(t) = Ae^{-s_1 t} + Be^{-s_2 t}[\alpha \sin\omega_3 t - \cos\omega_3 t]$$

$$+ Ce^{-s_4 t}[\cos\omega_5 t + \gamma \sin\omega_5 t] - De^{-s_r t}(1+f_1 t)\ . \quad (6)$$

A=66.6347, B=3.5306, C=0.06896, D=63.1731 amps; α= 8.71506, γ=21.0235; s_1=9.73703, s_2=1.19358, ω_3=0.344532, s_4=0.0471125, ω_5=0.0721595, s_r=11.1111, f_1=1.07665 GHz. Note that the adjusted network of Fig. 8a adds a fifth pole to the current expression, and thus it needs only two rise time poles

for i‴(0)=0. A double pole with 90 psec time constant (β=11.1111 GHz), or Elmore delay of 180 psec for the soft step function, was chosen.

IV. Field Pickup by Microstrip Board Lines

As discussed in the Introduction, IEC current Criterion (4) requires third time derivative i‴(0)=0 so that field derivatives dE/dt and dH/dt smoothly start up from zero. This is important for calculating any detector response and for calculating noise induced on PC board microstrip lines. Indeed, the latter can be used as field detectors by looking at sum and difference currents, as discussed by the author in [4]. If the geometry is simple enough (Figures 9-10a), calculating noise induced on microstrip lines due to a nearby IEC zap to ground involves (1) computing the E and H fields at each electrically small line segment, and (2) finding the line response in terms of 50-ohm waves launched into each direction on the lines, in accordance with formulae in [4]. These waves are summed with correct propagation delays and the predicted signal is found. Figure 9 shows a PC board with a 50-ohm trace (20 cm long) to SMA connectors at each end (50-ohm termination near the gun and 50 ohm cable at the opposite end), with board ground available near the line. The IEC gun is shown applied at position A as shown in Fig. 10a, although it can be moved about. As shown in Fig. 10b, the response to E-field steps (capacitive) is to send two equal charge packets in opposite directions on the microstrip, and for H-fields (inductive) the response is opposite-signed charge packets so that current is in a single direction and there is zero total charge transfer. This is why a microstrip field derivative detector is formed by tracking sum and difference currents on a short line segment [4].

The E and H fields turn out to be adequately represented by five dipoles of 1 cm length each (5 cm is the IEC probe length [1]), as pictured in Fig. 10a. The fields can then be computed as in Wilson and Ma [9] or, equivalently, as in the author's own pulsed Hertzian dipole work [10]. The currents are mirrored in the ground plane and appropriate propagation delays are applied to the dipoles. For these calculations, the IEC current expression as in [6] was used, which as noted earlier does satisfy Criterion (4).

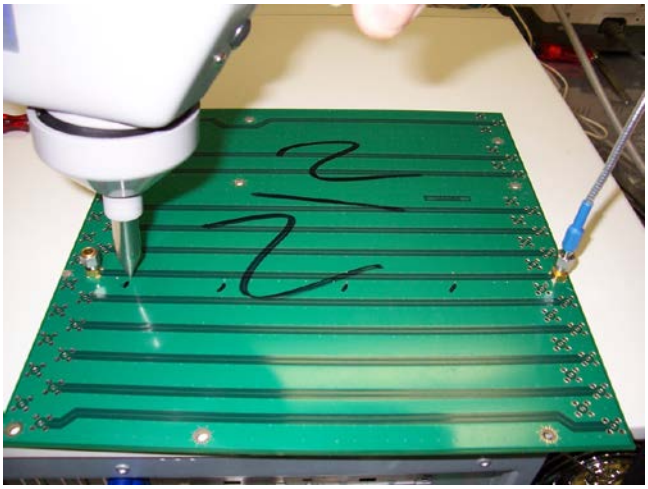


Figure 9: Printed circuit board with 50-ohm trace, terminated at each end. IEC gun pulse can be applied to exposed ground anywhere near the trace or at step displacements.

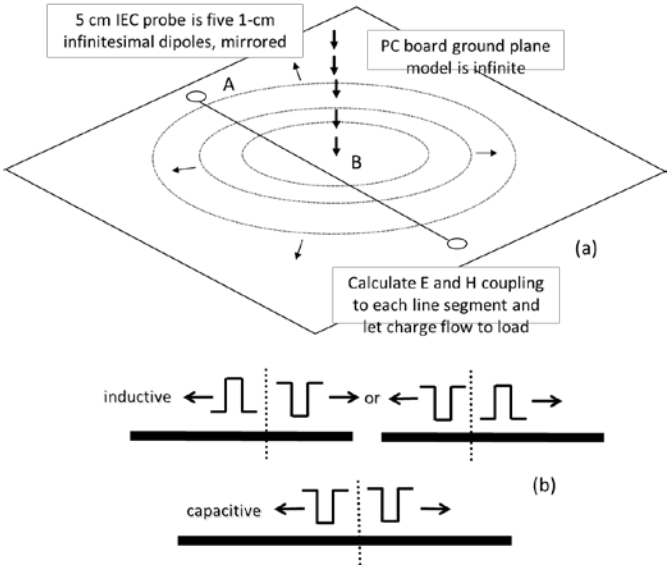
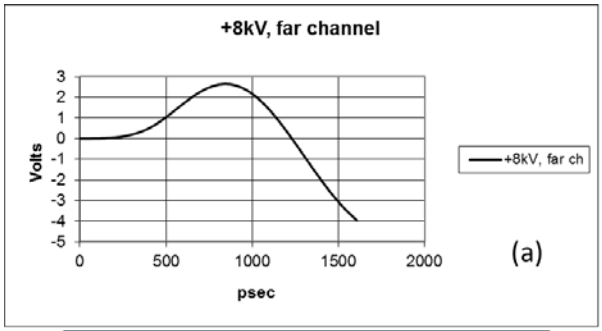


Figure 10: (a) Geometric scheme for calculation of IEC gun pulse to ground; Fig. 9 setup would have pulse source at point A. (b) Line segment charge flow as caused by H (inductive) or E (capacitive) fields.

The objective is to see if these simple calculations (tracked on an Excel spreadsheet) can roughly predict the magnitude, sign and timing of noise induced on a PC board line during a rather harsh open-chassis IEC zap to ground. The advantage to looking at the early part of a pulse is that complications such as multiple reflections from the board edges have not had time to take place. The general approach seems confirmed by recent related studies such as Shall, et al. [11], who studied the microstrip victim for a continuous wave source, but who also built a model with dipoles, ground mirror currents and simple microstrip formulae.

Our results are fairly good, considering the model's simplicity and relative ease of execution. Figure 11 shows the situation of Fig. 9, where the pulse source is at one end of the line (point A) and the signal is picked up at the far end. Magnitude, polarity, and time scale of the computed and detected signals are all within range of one another. The dominant initial signal is the expected positive current in response to H-field flux through the line. It was pointed out in [9] that the initial and final conditions of the static E-field are not always clear and must be chosen in order to get the total picture. In our case it appears that there is collapse of an initial dipole (there is a helpful related discussion in [10]), and thus a net flow of negative charge from the line when a +8kV IEC pulse is applied nearby; that is why negative charge flow from segments is pictured in Fig. 10b for E-fields. But the complete calculation also adds in the other dipole E-field components, which depend on time derivatives of the current, as fully discussed in [9-10].



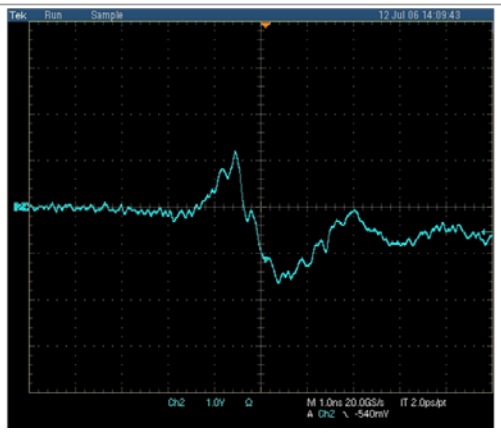
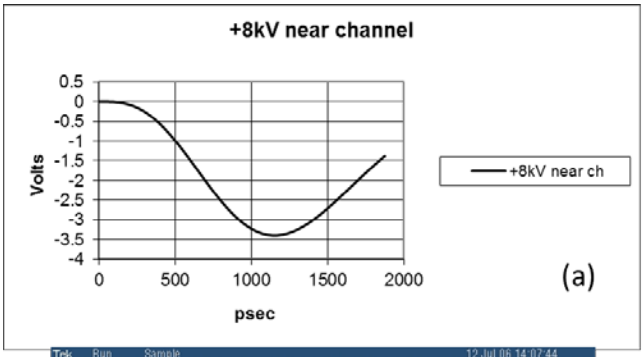


Figure 11: (a) Calculated far end signal for +8kV IEC pulse applied at point A. (b) Measured far end signal. Scope set at 1V/div, 1 nsec/div.

Figure 12 shows the situation of Fig. 9 with the 50-ohm cable and 50-ohm termination exchanged, i.e., pulse still applied at point A but with signal pickup on the near end. The measured signal is negative but so is the prediction—now both E-field and H-field responses are expected to be predominantly negative, in order to oppose line flux and to drive off initial negative line charge. Again, we achieve good qualitative agreement and reasonable quantitative agreement. Figure 13 shows the case of IEC gun zap applied in the middle of the board (point B), with signal measured at either end and expected to be equal due to symmetry. The measurement is not very different from the "far end" case of Fig. 11and shows the expected positive H-induced current once again.



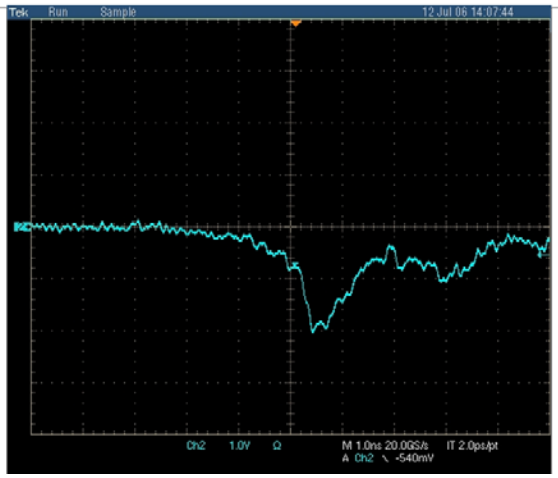


Figure 12: (a) Calculated near end signal for +8kV IEC pulse applied at point A. (b) Measured near end signal. Scope set at 1V/div, 1 nsec/div.

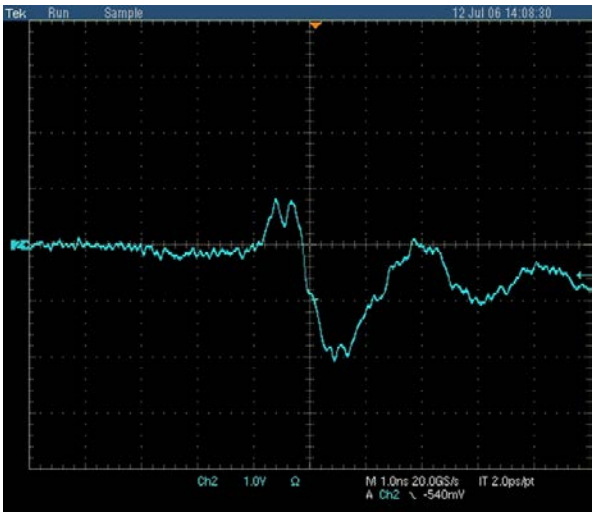


Figure 13: Measured signal from +8kV IEC pulse applied at point B, middle of board. Scope set at 1V/div, 1 nsec/div.

To the extent that the entire board serves as a field detector for E- and H-fields generated by the IEC gun, Figure 14 shows dE/dt and dH/dt as measured by calculated sum and difference currents of a zap applied at point A or equivalent (one must avoid the balanced H-field effects of a zap in the middle of the board, as the difference signal should be zero). This illustration separates the effects of Lenz's Law and Gauss's Law, as more fully discussed in [4].

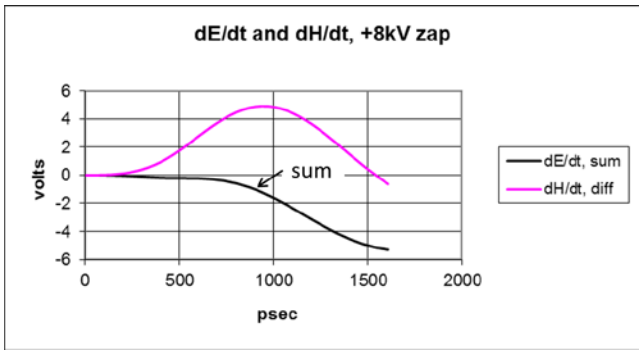


Figure 14: Calculated field derivatives from +8kV IEC pulse applied at point A, resulting from sum and difference currents on a 20 cm line. The effective dH/dt reaches zero a reasonable propagation time after the IEC pulse peak current.

V. Discussion and Conclusion

We have described a revised circuit model for the IEC 61000-4-2 ESD pulse, one that maps directly to a new compact analytic expression for the short-circuit current waveform. It meets and exceeds all aspects of the IEC waveform as specified in the 61000-4-2 document [1]. Unlike other unified models, this one uses a simply-expressed nonideal step voltage function to allow E and H-field derivatives to be initialized at zero. The latter then allows calculated radiated noise pickup signals to be free of unphysical results like steps and impulses.

The IEC pulse coupled to a platform by series capacitance [2] could become familiar enough that we want to capture the series capacitance in the pulser and thus allow a simpler ground return to the component, board, or platform under test. For that reason we have presented a series capacitive tool that fits onto an IEC pulser, for the purpose of forming such a pulse. An IEC-like pulse as modified by series capacitance also appears to happen to I/O port pins, under use conditions such as the unshielded flash drive. This further motivates the development and use of the capacitive coupling tool for the IEC pulser. As expected the initial IEC current spike is largely preserved, and the trailing pulse is attenuated. However the higher impedance of the series capacitance brings out at least one additional circuit element, a bypass capacitance from pulser gun directly to ground. This diverts some current from the load for these higher impedances, yet has little or no effect on the near-short conditions of the waveform spec in [1]. It is not known if this bypass capacitance varies with the physical size of the IEC pulser, as would be expected. That should be studied further, as should other high-impedance loads such as higher resistance. In the present studies it became clear that only a "certified" IEC 61000-4-2 setup meeting all expectations of [1] could give consistent, explainable results for the higher impedance loads.

Field-induced signals arise in board traces due to electric and magnetic field coupling to the IEC pulser gun when zaps are applied to the board (or chassis) ground plane nearby. These are thought to be a major source of noise-induced faults during IEC pulse testing of systems, yet calculations of the expected effects, even under idealized conditions, have been rare. This work began with IEC current expressions suitable for physically meaningful initial field derivatives of zero. Such an expression was used to calculate electric and magnetic flux impinging on line segments, and to compute their current flow effects, following earlier methods [4]. These spreadsheet-level calculations compared favorably to measured cases of a microstrip line victim and an IEC pulse applied to the PC board ground nearby.

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References

[1] IEC 61000-4-2 System ESD specification, Edition 2.0, 2008.

[2] A. Tazzoli, S. Malobabic, V. Vashchenko, "Modeling of the Text-Fixture/Horizontal Coupling Plane Interaction in System-Level ESD Test Setups", 2014 EOS/ESD Symposium Proceedings, pp. 154-160.

[3] ANSI/ESD SP5.6 Human Metal Model (HMM)--Component Level, 2009.

[4] T.W. Chen, T.J. Maloney, and B. Chou, "Detecting E and H Fields with Microstrip Transmission Lines", 2008 EMC Symposium, August 2008.

[5] R. Mertens, H. Kunz, A. Salman, G. Boselli, and E. Rosenbaum, 2012 EOS/ESD Symposium Proceedings, pp. 373-78.

[6] K. Wang, D. Pommerenke, R. Chundru, T. Van Doren, J. L. Drewniak, A. Shashindranath, “Numerical Modeling of Electrostatic Discharge Generators”, IEEE Trans. Electromagnetic Compatibility, 45, pp. 258-271 (2003).

[7] K. Wang, J. Wang, X. Wang, "Four Order Electrostatic Discharge Circuit Model and its Simulation", TELKOMNIKA, Vol.10, No.8, December 2012, pp. 2006-12.

[8] T.J. Maloney, “Primary and Induced Currents from Cable Discharges”, 2010 IEEE EMC Symposium, July 2010, pp. 686-691.

[9] P.F. Wilson and M.T. Ma, "Fields Radiated by Electrostatic Discharges", IEEE Trans. Electromagnetic Compatibility, 33, Feb. 1991, pp. 10-18.

[10] T.J. Maloney, "Easy Access to Pulsed Hertzian Dipole Fields Through Pole-Zero Treatment", cover article, IEEE EMC Society Newsletter, Summer 2011, pp. 34-42.

[11] H. Shall, Z. Riah, and M. Kadi, "A Novel Approach for Modeling Near-Field Coupling With PCB Traces", IEEE Trans. Electromagnetic Compatibility 56, Oct 2014, pp. 1194-1201.