

# Low Impedance Contact CDM

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**Abstract** – Relay-based contact CDM (CCDM) is shown to closely replicate the waveforms and failure currents of legacy field-induced CDM when the effective system impedances are approximately matched. The repeatability of the waveforms will be crucially important as CDM test levels decrease below 250 V. Recommendations for inclusion in future standards are presented.

## I. Introduction

In an effort to replicate the stress conditions present in an automated manufacturing environment, the standardized field-induced CDM tester (FICDM) [1] relies on an air spark to generate the ESD event. The air spark is inherently variable and dependent upon many factors. The result is a “standard” which produces significant zap-to-zap variation [2]. To-date this variation has been tolerated as a necessary tradeoff to avoid the negative consequences that often accompany alternative test methods, such as the parasitic capacitance of socketed CDM [3].

When testing below the widely adopted qualification level of 250 V, FICDM variability transitions from inconvenient to intolerable. Figure 1 shows the maximum to minimum difference in  $I_{\text{peak}}$  (top) and the standard deviation (bottom) as a percentage of the average  $I_{\text{peak}}$  of 50 zaps to calibration coins. Below 250 V, the variation in  $I_{\text{peak}}$  as a percentage of the mean increases as the precharge voltage  $V_{\text{pre}}$  decreases. The data in Figure 2 reveal that while the maximum  $I_{\text{peak}}$  is linearly proportional to  $V_{\text{pre}}$ , the minimum  $I_{\text{peak}}$  is not. Runt pulses are increasingly common and the attenuation more severe as the  $V_{\text{pre}}$  decreases, which in turn decreases the mean.

To satisfy scaling and circuit performance demands of the near future, components designed for less than 250 V CDM will become commonplace [4], [5]. The CDM protection levels for non-exposed intra-package I/Os (e.g., through-silicon vias) is likely to be well below 100 V CDM [5]. A repeatable, reproducible alternative to FICDM must be adopted to prevent a significant increase in the testing and design time wasted to accommodate a highly variable standard.

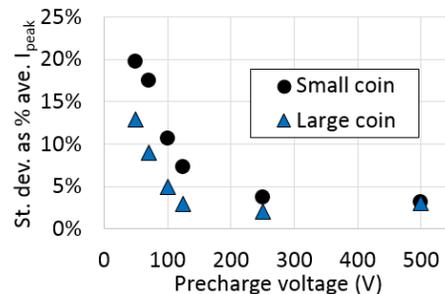
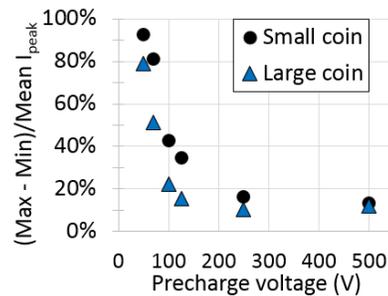


Figure 1:  $I_{\text{peak}}$  maximum - minimum (top) and the standard deviation (bottom) of 50 zaps to JEDEC calibration coins as a percentage of the mean; 26% relative humidity. Data taken on an Orion2 FICDM system using an 8 GHz oscilloscope.

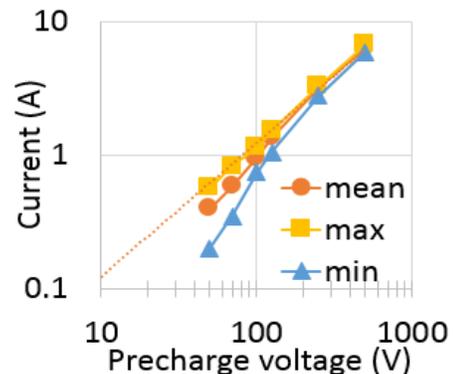


Figure 2: Maximum, minimum, and mean  $I_{\text{peak}}$  as a function of  $V_{\text{pre}}$  when stressing the small JEDEC coin.

Relay-driven contact CDM testers (CCDM) such as capacitively coupled TLP (CC-TLP) [6] and Thermo Fisher’s “CDM2” [2] have been proposed to eliminate the air spark and improve repeatability. However, the decay constant of these 50  $\Omega$  systems results in pulses wider than those of FICDM, introducing a potential source of miscorrelation as will be shown. The rise time  $t_{rise}$  of CCDM can also be significantly faster than FICDM [2] and can cause a miscorrelation in ICs where rise-time-sensitive protection devices are used (e.g., SCRs).

In this work, CCDM testers with reduced system impedance are presented. The new testers generate waveforms more closely resembling those of FICDM than their 50  $\Omega$  predecessors. Equivalent RLC models for the various testers are produced and compared. Failure correlation from a 14nm bulk finFET test chip containing various I/O types and protection devices is presented. Finally, a proposal is made for accommodating CCDM testers in future revisions of the CDM standard.

## II. CCDM Tester Variations

CDM testers can be well approximated as an equivalent series RLC circuit [7]. The pulse width is an increasing function of the effective discharge resistance  $R_{eff}$  and capacitance  $C_{eff}$ . The  $R_{eff}$  of existing 50  $\Omega$  CCDM testers will nearly always exceed that of FICDM, which can be as low as 24  $\Omega$  [7]. Consequently, reducing the system impedance of CCDM should result in better waveform matching to FICDM.

In this section, CCDM testers with system impedances of 50  $\Omega$ , 25  $\Omega$ , and 11  $\Omega$  are described.

### A. 50 $\Omega$ CCDM

To-date, package-level 50  $\Omega$  CCDM has been instantiated in two primary forms: CC-TLP [6] and CDM2 [2]. Both are reviewed briefly here.

CC-TLP, illustrated in Figure 3, is essentially a 50  $\Omega$  VF-TLP tester with an FICDM-like test head. The VF-TLP pulse is applied at the pogo pin; the return path is the effective capacitance of the device under test (DUT) to the ground plane. A bipolar stress is delivered as displacement current charges and discharges the DUT during the pulse rising and falling edges, respectively. The current is extracted from the incident ( $V_{inc}$ ) and reflected ( $V_{DUT}$ ) voltage waveforms as in TDR VF-TLP:

$$I_{DUT}(t) = \frac{V_{inc}(t) - V_{DUT}(t)}{50 \Omega} . \quad (1)$$

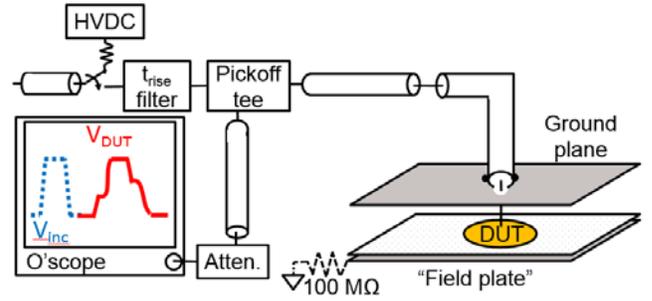


Figure 3: 50  $\Omega$  CC-TLP tester. The field plate resistor is not present in existing CC-TLP literature, but it can be added (as is done in CDM2) to more closely mimic the FICDM system.

CDM2 is illustrated in Figure 4. With the pogo pin contacting the DUT, the effective  $C_{DUT}$  and the coaxial cable leading to it are slowly charged. A relay then quickly discharges the system to ground through a 50  $\Omega$  coaxial cable and oscilloscope channel. This generates a unipolar current stress in the DUT. The current extraction is the same as for CC-TLP; see Equation (1).  $V_{inc}$  is the discharge with no DUT, and  $V_{DUT}$  is the discharge when contacting the DUT.

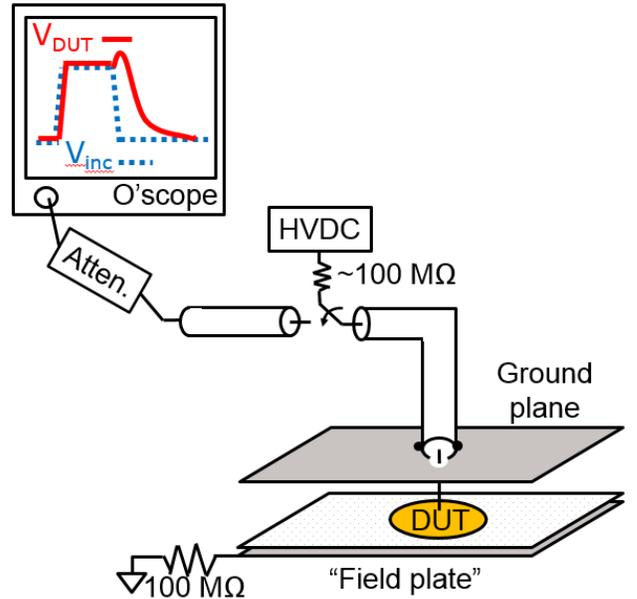


Figure 4: 50  $\Omega$  “CDM2” tester used in this work, as in [2].

Fundamentally CC-TLP and CDM2 are the same: both utilize a 50  $\Omega$  relay and transmission line to charge and/or discharge the device. Consequently the RC decay constant of the discharge to a given DUT is the same for both testers, provided the dimensions of the test head and field plate are the same.

In this work, a Thermo Fisher CDM2 tester was selected to represent the 50  $\Omega$  CCDM testers, chosen for its commercial availability and unipolar stress.

## B. 25 $\Omega$ CCDM

The system impedance of CCDM can be halved by connecting a parallel 50  $\Omega$  coaxial cable to the discharge path. This is illustrated in Figure 5. The system resembles a TDT VF-TLP system [8] whose pulse is applied to a CDM test head. A 200ps  $t_{\text{rise}}$  filter is used to achieve a  $t_{\text{rise}}$  comparable to that of FICDM – an advantage over CDM2. Similar to CC-TLP, displacement current stresses the device on the pulse rising and falling edges. To enable unipolar stress, the charge cable is terminated with an RC network. R is chosen to be 50  $\Omega$  to suppress reflections, and C is set to 10 nF. The resulting 500 ns RC time constant is slow enough to eliminate any significant displacement current in the DUT during the pulse falling edge.

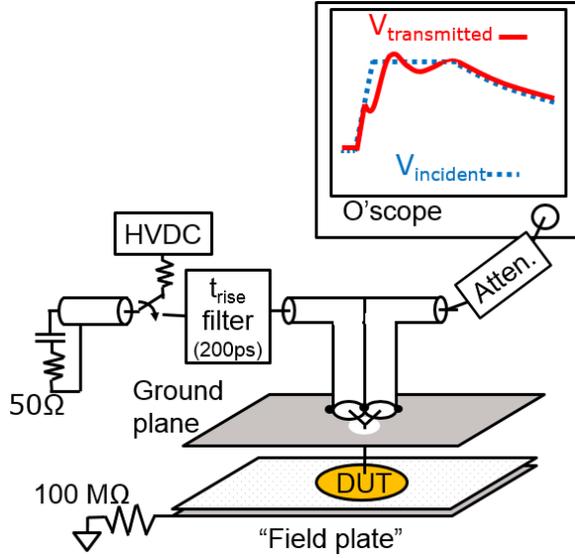


Figure 5: Illustration of the 25  $\Omega$  CCDM tester used in this work, which resembles a TDT VF-TLP system injecting into a CDM test head. The RC termination of the charge cable ensures a single-polarity stress.

The device current extraction is similar to that of a TDT VF-TLP system (see Appendix A for more on  $I_{\text{DUT}}$  extraction). From transmission line theory,

$$I_{\text{DUT}}(t) = \frac{V_{\text{inc}}(t) - V_{\text{reflected}}(t) - V_{\text{transmitted}}(t)}{50 \Omega}. \quad (2)$$

$V_{\text{transmitted}}$  is the voltage measured directly at the oscilloscope when in contact with the DUT.  $V_{\text{inc}}$  can also be measured at the oscilloscope when the pogo pin is separated from the DUT. By observing that

$$V_{\text{transmitted}}(t) = V_{\text{inc}}(t) + V_{\text{reflected}}(t), \quad (3)$$

Equation (2) simplifies to

$$I_{\text{DUT}}(t) = \frac{V_{\text{inc}}(t) - V_{\text{transmitted}}(t)}{25 \Omega}. \quad (4)$$

## C. 11 $\Omega$ CCDM

The CCDM system impedance can be further reduced to below 25  $\Omega$ . One approach would be to add a third, fourth, or even fifth coaxial cable in parallel with the two that lead to the pogo pin in the 25  $\Omega$  system. As long as each is terminated with 50  $\Omega$ , the system impedance seen by the device is equal to 50  $\Omega$  divided by the total number of cables. Alternatively, a surface mount resistor can be soldered across the center and ground conductors near the pogo pin. In this work, a 20  $\Omega$  resistor with low parasitics is used. This is illustrated in Figure 6. The tester is otherwise identical to the 25  $\Omega$  system in Figure 5. The effective system impedance is now  $20 \parallel 50 \parallel 50 \Omega = 9/100 \Omega = 11.11 \Omega$ .

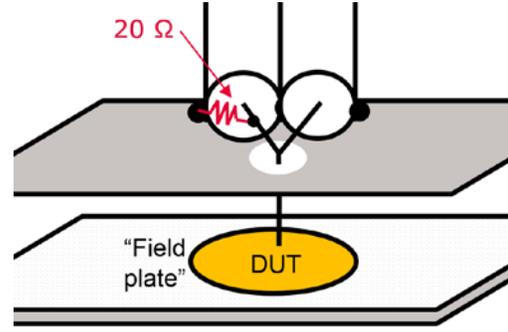


Figure 6: Zoomed-in illustration of 11  $\Omega$  CCDM. The tester is identical to 25  $\Omega$  CCDM with the addition of a 20  $\Omega$  surface mount resistor soldered across the center and shield conductors near the pogo pin.

The device current is as in Equation (2), with an additional 20  $\Omega$  path that must be accounted for:

$$I_{\text{DUT}}(t) = \frac{V_{\text{inc}}(t) - V_{\text{reflected}}(t) - V_{\text{transmitted}}(t)}{50 \Omega} - \frac{V_{\text{transmitted}}(t)}{20 \Omega}. \quad (5)$$

By substituting Equation (3), Equation (5) becomes

$$I_{\text{DUT}}(t) = \frac{4 \cdot V_{\text{inc}}(t) - 9 \cdot V_{\text{transmitted}}(t)}{100 \Omega}. \quad (6)$$

Unlike 25  $\Omega$  CCDM, the waveform measured at the oscilloscope with the pogo separated from the DUT is not  $V_{\text{inc}}$ . Rather, it is a reference waveform  $V_{\text{rfr}}$ :

$$V_{\text{rfr}} = V_{\text{inc}}(1 + \Gamma). \quad (7)$$

In Equation (7),  $\Gamma$  is the reflection coefficient for the incident pulse when it reaches the  $20 \parallel 50 \Omega$  branch. By substituting Equation (7) into (6), one obtains

$$I_{\text{DUT}}(t) = \frac{9 \cdot V_{\text{rfr}}(t) - 9 \cdot V_{\text{transmitted}}(t)}{100 \Omega} = \frac{V_{\text{rfr}}(t) - V_{\text{transmitted}}(t)}{11.11 \Omega}. \quad (8)$$

### III. Discharge Waveform Analysis

In this section, discharge waveforms from the three CCDM systems described in Section II are compared against FICDM. All three CCDM systems were implemented using modifications of the CDM2 Orion2 tester by Thermo Fisher [2]. All physical dimensions of each tester (e.g., ground plate size and field plate dielectric) conform to the JEDEC standard [1]. An 8GHz oscilloscope was used for all waveform measurements in this work.

#### A. Waveform Comparison

Discharge waveforms from FICDM and CCDM zaps to JEDEC calibration coins are shown in Figure 7. As expected, CCDM more closely replicates FICDM when the system impedance is reduced. Only the 11  $\Omega$  CCDM system can generate an underdamped waveform on both coins like FICDM. The pulse base width of the 50  $\Omega$  discharge is significantly wider than that of the legacy tester, especially when zapping the larger coin.

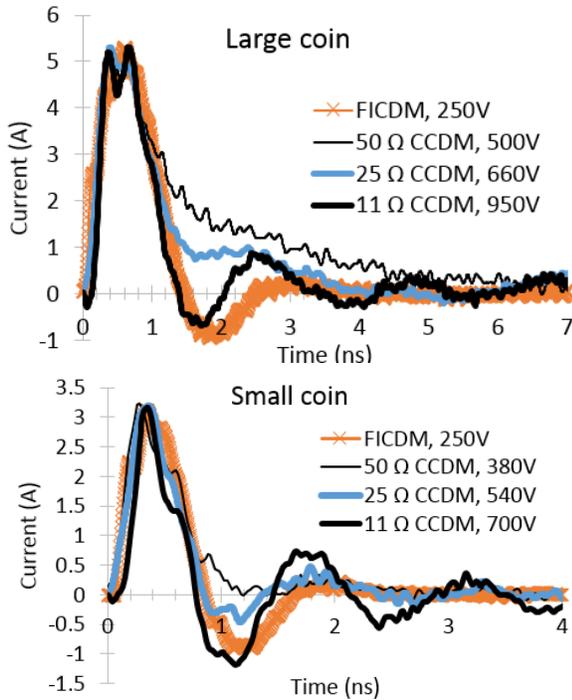


Figure 7: Discharge waveforms from FICDM and CCDM zaps to JEDEC large and small calibration coins.

Put another way, the total charge  $Q_{tot}$  delivered for a given  $I_{peak}$  increases with the system impedance. This is shown in Figure 8, where  $I_{peak}$  is plotted as a function of  $Q_{tot}$  using four calibration coins of different sizes. In the case of the largest coin, the  $Q_{tot}$  per  $I_{peak}$  is more than double that of FICDM. The 25  $\Omega$  system comes closer to approximating FICDM, while

the 11  $\Omega$  system matches quite well. For the smallest coin, the discharge from the 11  $\Omega$  system actually has slightly less charge per  $I_{peak}$  than FICDM. This suggests that a slightly larger system impedance – like 16  $\Omega$  – might result in the best overall match.

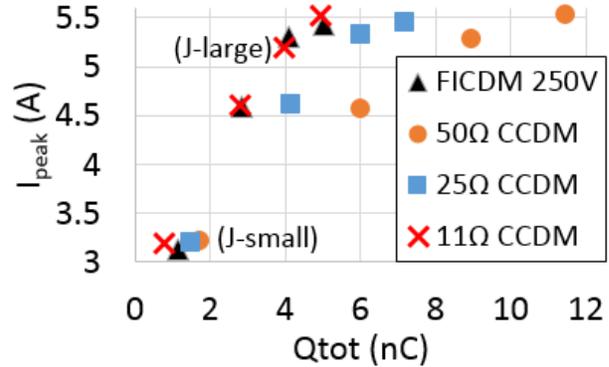


Figure 8: Total charge delivered to obtain a given  $I_{peak}$  when stressing four calibration coins of different size.

It has been proposed that the pulse width of a 50  $\Omega$  CC-TLP system could be artificially reduced by applying, for example, a 1 ns VF-TLP pulse to the system rather than a 10 – 20 ns pulse. While this would limit the duration of the stress associated with the VF-TLP pulse rising edge, it also makes the pulse width approximately independent of  $C_{DUT}$ . This is undesirable if CCDM is to replicate FICDM; the latter clearly exhibits pulse width dependence on  $C_{DUT}$  (see Figures 7 – 8). Low impedance CCDM can capture this  $C_{DUT}$  dependence and replicate the legacy  $Q_{tot}$  per  $I_{peak}$ .

#### B. System RLC models

Equivalent 2-pole RLC models derived from the discharge waveforms can lend significant insight into waveform correlation with FICDM [7]. The models derived from the waveforms in Figure 7 are listed in Table 1. The  $C_{eff}$  for a given coin is constant across testers – the required outcome since all testers use the same field and ground plates. The commercial FICDM test head contained a ferrite disk (not prohibited in the 2013 JEDEC standard [1]), while CCDM uses no ferrites. This results in a lower inductance  $L_{eff}$  for CCDM in all cases [7].

Table 1: 2-pole RLC models derived from the discharge waveforms of Figure 7.

	Large coin			Small coin		
	$R_{eff}$ ( $\Omega$ )	$L_{eff}$ (nH)	$C_{eff}$ (pF)	$R_{eff}$ ( $\Omega$ )	$L_{eff}$ (nH)	$C_{eff}$ (pF)
FICDM	27.0	9.9	16.4	34.1	11.2	4.8
11 $\Omega$ CCDM	26.6	6.1	16.6	18.7	6.0	4.7
25 $\Omega$ CCDM	53.0	6.2	16.6	53.5	6.6	4.9
50 $\Omega$ CCDM	85.0	6.1	16.4	70.5	6.8	4.9

The primary differentiator among the testers is  $R_{\text{eff}}$ , the largest component of which is the characteristic impedance of the system. The  $R_{\text{eff}}$  of 50  $\Omega$  CCDM with the large coin is more than three times that of FICDM, resulting in a wide discharge pulse. The excellent waveform match of 11  $\Omega$  CCDM to FICDM is primarily due to the close agreement of  $R_{\text{eff}}$ . Table 1 also indicates that the dependence of  $R_{\text{eff}}$  on coin size (i.e.  $C_{\text{DUT}}$ ) is opposite between FICDM and CCDM:  $R_{\text{eff}}$  decreases with  $C_{\text{DUT}}$  for CCDM while the reverse is true for FICDM. So, while the  $R_{\text{eff}}$  of 11  $\Omega$  CCDM matches FICDM for the large coin, it is somewhat low for smaller DUTs. This further supports the idea that a CCDM system impedance somewhere between 11  $\Omega$  and 25  $\Omega$  would likely result in the best overall fit.

Because CCDM is mercury-relay driven, the repeatability is excellent, as shown in Figure 9 for the 25  $\Omega$  system.

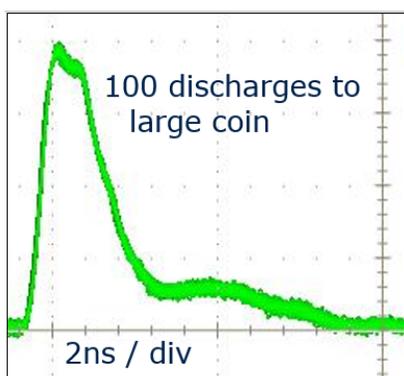


Figure 9: Waveforms of 100 discharges to the large calibration coin using 25  $\Omega$  CCDM.

### C. $I_{\text{peak}}$ dependence on $V_{\text{pre}}$ and $C_{\text{eff}}$

The  $I_{\text{peak}}$  generated for a given power supply voltage  $V_{\text{pre}}$  varies significantly among the testers, as shown in Figure 10. FICDM generates at least twice as much current per  $V_{\text{pre}}$  than the CCDM testers. This is due to differences in the stress generation methods.

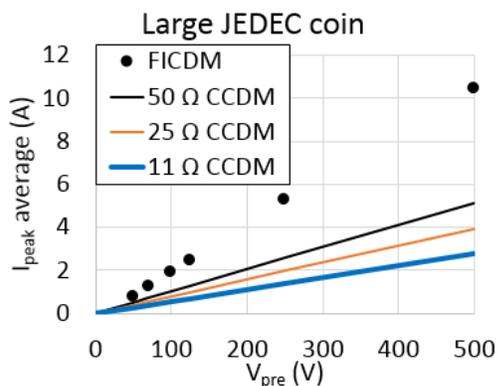


Figure 10:  $I_{\text{peak}}$  for a given  $V_{\text{pre}}$  when stressing the large JEDEC coin.

During FICDM, the potential of the DUT is nearly equal to  $V_{\text{pre}}$  just before the spark pulls it to ground potential; i.e., nearly the full  $V_{\text{pre}}$  generates the current stress. This is not the case for CCDM.  $V_{\text{pre}}$  is applied initially to the charge cable (terminated by  $C_{\text{DUT}}$  in 50  $\Omega$  CDM2). When the relay closes,  $V_{\text{pre}}$  is divided equally across the two 50  $\Omega$  coaxial cables on either side of the relay. This results in a square pulse of amplitude  $V_{\text{pre}} / 2$  that travels away from the charge cable, and a  $-V_{\text{pre}} / 2$  pulse that travels towards the end of the charge cable. In CDM2 the  $-V_{\text{pre}} / 2$  pulse in the charge cable is superimposed upon the static  $V_{\text{pre}}$  that was initially present across  $C_{\text{DUT}}$ . In CC-TLP and 25  $\Omega$  – 11  $\Omega$  CCDM, the  $V_{\text{pre}} / 2$  pulse travels towards the DUT. In other words, in both CDM2 and CC-TLP-type systems it is the transition from  $V_{\text{pre}}$  to  $V_{\text{pre}} / 2$  across  $C_{\text{DUT}}$  that initiates the current stress (see Appendix A for further discussion). This is approximately half of the voltage involved in the FICDM stress generation and hence generates approximately half the  $I_{\text{peak}}$  of FICDM. In the 25  $\Omega$  and 11  $\Omega$  case, the current from the  $V_{\text{pre}} / 2$  pulse is further diverted from the DUT to ground through the additional parallel paths connected near the pogo pin (see Figures 5 and 6). Hence, the  $I_{\text{DUT}}$  per  $V_{\text{pre}}$  is even lower in these systems than in 50  $\Omega$  CCDM.

$I_{\text{peak}}$  is also a function of the device capacitance; however, this dependency is not the same between FICDM and CCDM. As shown in Figure 11, FICDM  $I_{\text{peak}}$  is more strongly modulated by  $C_{\text{eff}}$  than is CCDM. This means that while  $V_{\text{pre}}$  can be adjusted to match the  $I_{\text{peak}}$  of CCDM to FICDM for a given  $C_{\text{eff}}$ , this same  $V_{\text{pre}}$  will not produce a matched  $I_{\text{peak}}$  for a different  $C_{\text{eff}}$ .

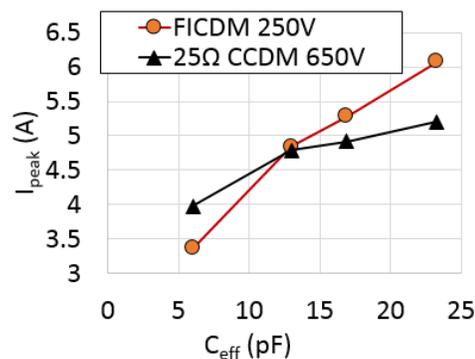


Figure 11:  $I_{\text{peak}}$  dependence upon  $C_{\text{eff}}$  for FICDM and 25  $\Omega$  CCDM. The data is from zaps to calibration coins of four different sizes at the FICDM equivalent of 250 V.

Given the different dependencies of  $I_{\text{peak}}$  on  $V_{\text{pre}}$  and  $C_{\text{eff}}$ ,  $I_{\text{peak}}$  must be used rather than  $V_{\text{pre}}$  to correlate the results. Section V contains suggestions for accommodating these differences in a future standard.

## IV. Test Chip Correlation

The testers discussed in Section II were used to stress the I/Os of a 14 nm bulk finFET [9] test chip. The test chip and the measurement results are discussed in this section.

### A. Test Chip Description and Discharge Waveforms

The test chip utilizes dual diode protection at the I/Os with an RC triggered PMOS clamp between the power rails. Two different I/O architectures are used on the chip, and the sizes of the ESD diodes are varied. The test chip is packaged in a large 38 mm by 38 mm LGA package with heat sink. Because pulse width dependence is more pronounced with larger DUTs (see Figure 7), this large package should exacerbate any miscorrelation arising from pulse width. Indeed, the discharge waveforms from the test chip, shown in Figure 12, reveal a significant pulse width dependence on tester impedance.  $T_{rise}$  is approximately matched across the systems, though that of CDM2 is approximately 50 ps sharper than the others. Wafer-level characterization indicates these I/Os are not sensitive to  $t_{rise}$ , so any miscorrelation should arise from differences in  $t_{width}$ .

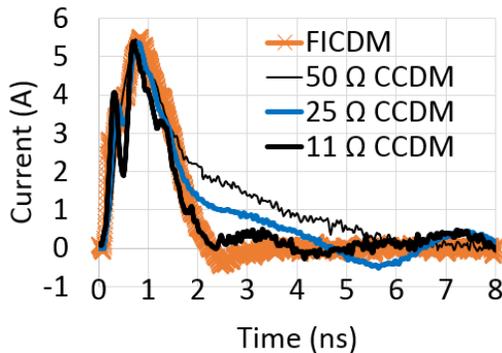


Figure 12: Discharge waveforms from the test chip used in this work.

### B. $I_{peak}$ vs. Pin Location

While  $Q_{tot}$  is independent of I/O pin location in the package during FICDM testing,  $I_{peak}$  and  $t_{width}$  are location dependent [10]. Waveforms from pins near the center have a larger  $I_{peak}$  and shorter  $t_{width}$  than those from pins near the package edge (charge across the package must travel longer distances to reach an edge discharge point). This source of variation is an important one for CCDM to capture if it is to replicate FICDM failures.

The I/O peak currents measured during FICDM and CCDM are mapped by pin location in Figure 13. The

trend of larger  $I_{peak}$  in the center vs. the edges holds true for CCDM. This is an expected but important observation for ensuring correlation with FICDM  $I_{fail}$ .

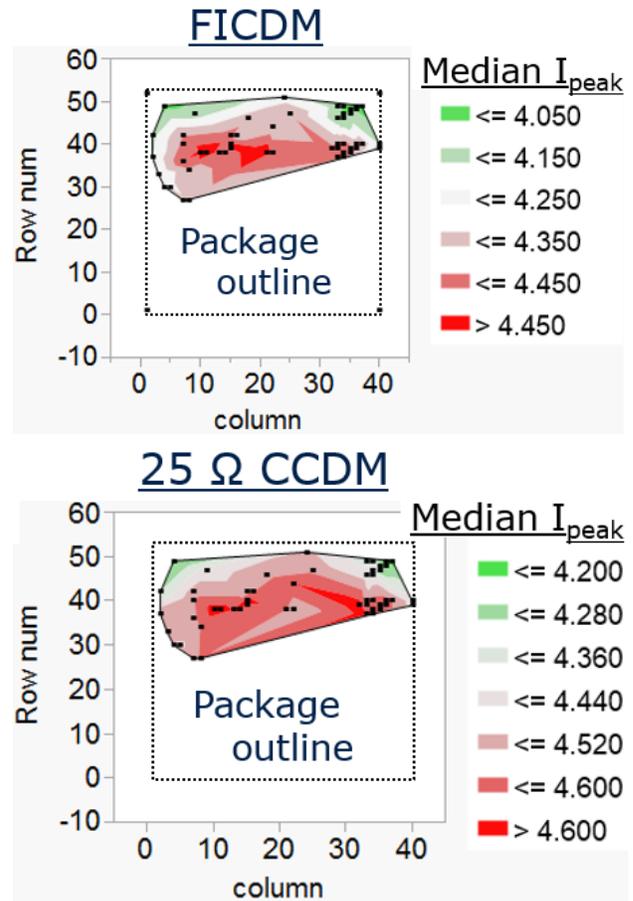


Figure 13: Map of  $I_{peak}$  by I/O pin location on both FICDM and CCDM taken at the FICDM equivalent of 250 V.

### C. $I_{fail}$ Correlation

Three test chip samples per CDM tester type were stressed and the failure currents recorded for several pins. All testers were configured to generate positive current stress into the pin – the worst case stress condition for this test chip. Failure was defined as a 4% post-stress deviation in an unpowered IV sweep of the pin. Because the low impedance CCDM testers produce less  $I_{peak}$  per  $V_{pre}$  than FICDM (see Figure 10), sufficient current could not be generated to cause failure in a few I/Os. Where failure was not achieved, the last passing current is reported.

The  $I_{fail}$  results are shown in Figures 14 and 15 for two different I/O types. For both I/O types, the wider pulses of 50  $\Omega$  CCDM result in  $I_{fail}$  values significantly below FICDM.  $I_{fail}$  for 25  $\Omega$  CCDM is typically lower than FICDM, but within 5%. The  $I_{fail}$  resulting from 11  $\Omega$  CCDM typically falls within the FICDM distribution, and in some cases it exceeds

FICDM. As discussed in Section III, it is likely that even better waveform and failure correlation could be obtained with a system impedance somewhere between 25  $\Omega$  and 11  $\Omega$ . Regardless, either of the lower-impedance CCDM testers are excellent candidates for successors to FICDM.

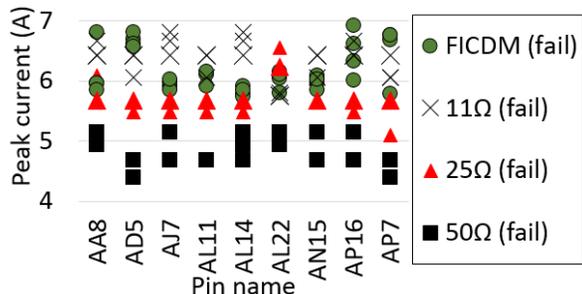


Figure 14: Failure current correlation for I/O type #1.

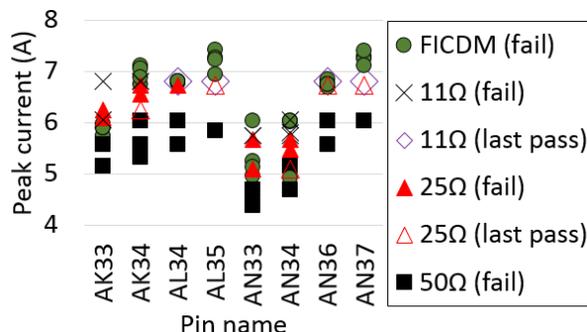


Figure 15: Failure current correlation for I/O type #2.

## V. Inclusion in Standards

Future CDM standards must allow the use of innovative FICDM alternatives such as CCDM. This can be achieved while preserving the legacy voltage classification levels, allowing both FICDM and CCDM to co-exist. If the following three properties of a tester match those of FICDM, the stress to the DUT should be identical:

Property 1: The distribution of charge across the DUT

Property 2: The  $I_{\text{peak}}$  delivered during the stress

Property 3: The waveform shape, including rise time, pulse width, and charge per  $I_{\text{peak}}$

Property 1 above can be guaranteed by specifying all test head and field plate dimensions, including the pogo pin length and field plate dielectric. The characteristics in Property 3 should be specified in terms of acceptable ranges when stressing specific calibration coins.

To achieve Property 2, CDM hardness should be quantified in terms of  $I_{\text{peak}}$  rather than  $V_{\text{pre}}$  (see Section III.C).  $V_{\text{pre}}$  then becomes a legacy “test

condition” rather than an actual measure of the field plate voltage, much as is done in the recent Joint CDM Standard [11].

Mapping between  $I_{\text{peak}}$  and the legacy  $V_{\text{pre}}$  can be achieved through a look-up table or continuous model, with  $V_{\text{pre}}$  and  $C_{\text{eff}}$  as input variables. It was shown in [7] that FICDM  $I_{\text{peak}}$  can be very accurately predicted with an RLC model.  $L_{\text{eff}}$  is approximately constant. The relationship between  $R_{\text{eff}}$  and  $C_{\text{eff}}$  is linear:

$$R_{\text{eff}} \cdot C_{\text{eff}} = R_0 \cdot C_{\text{eff}} + \tau a u_0. \quad (9)$$

The constants  $R_0$  and  $\tau a u_0$  are chosen empirically, leaving  $I_{\text{peak}}$  as a function of only two variables:  $V_{\text{pre}}$  and  $C_{\text{eff}}$ . This is illustrated in Figure 16, where the excellent fit to measurements on various calibration coins can be seen. The maximum  $I_{\text{peak}}$  rather than the average was used; arguably CCDM should be targeted to replicate the worst stress a device pin could feel on FICDM. This also simplifies the modeling since, for a given  $C_{\text{eff}}$ , the maximum  $I_{\text{peak}}$  is linear with  $V_{\text{pre}}$  while the average is not (see Figure 2).

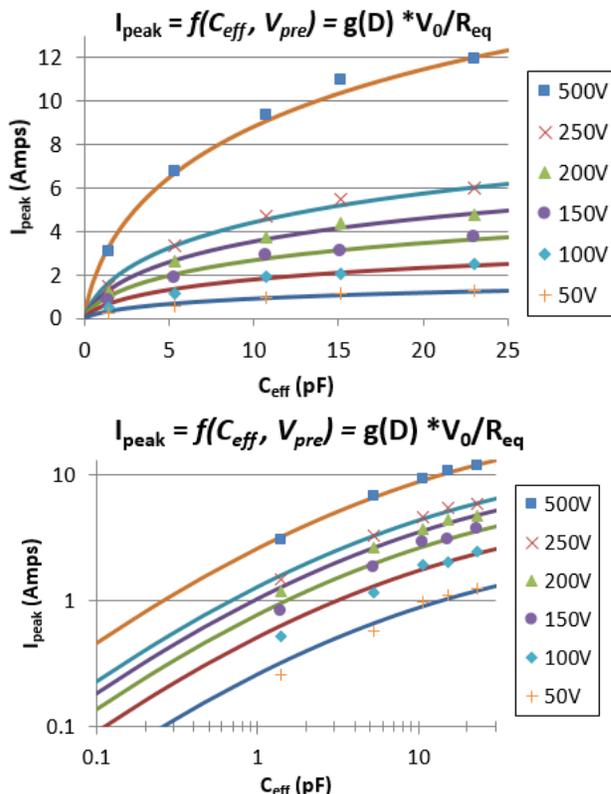


Figure 16: Solid lines: a continuous 2-pole model [7] of FICDM  $I_{\text{peak}}$  as a function of  $C_{\text{eff}}$  and  $V_{\text{pre}}$ , with  $L_{\text{eff}} = 11$  nH,  $\tau a u_0 = 85$  ps, and  $R_0 = 20$   $\Omega$ . Symbols: Maximum  $I_{\text{peak}}$  measured out of 50 zaps to metal coins of various sizes.

A CCDM test flow like the one proposed below would capture the dependencies embedded in the legacy FICDM voltage qualification levels:

1. Zap the  $V_{SS}$  pin of the largest domain on the product. Software integrates this waveform to determine  $C_{eff}$  automatically.
2. To test a part for a given  $V_{pre}$  robustness (e.g. “200 V CDM”), the  $C_{eff}$  from Step 1 is plugged into the continuous FICDM model of Figure 16 to obtain the targeted  $I_{peak}$ . Using the known  $I_{peak}$  per  $V_{pre}$  relationship of the CCDM tester for that  $C_{eff}$ , software automatically sets  $V_{pre}$  to achieve the  $I_{peak}$  specified as per Figure 16.
3. With  $V_{pre}$  now established, all pins are stressed.  $I_{peak}$  variation by pin location occurs naturally (an essential part of Property 2).
4. The results can either be reported in terms of legacy  $V_{pre}$  or  $I_{peak}$ , regardless of whether an actual FICDM tester or a CCDM tester was used.

## VI. Conclusions

Future CDM standards must allow the use of alternatives to FICDM. This will be especially crucial as qualification levels decrease below 250 V. A methodology for allowing co-existence of alternative testers with FICDM in future standards was presented. Such a standard will open the door for innovations in CDM tester design, the most promising of which is likely to be low impedance CCDM. The proposed methods for reducing the system impedance of CCDM result in excellent waveform and failure correlation to FICDM – a significant improvement over their 50  $\Omega$  predecessors. A broader correlation study involving multiple on-chip protection schemes, technology nodes, and IC suppliers should drive the ultimate selection of the CCDM system impedance adopted as an FICDM alternative.

### Appendix A: Extracting CCDM Device Currents

CCDM applies a step function to a matched transmission line with target load  $Z_L$  at its end, as pictured in Figure A.1. Current in the  $s$ -domain can be found from the input admittance at the step source,

$$\text{or } I(s) = \frac{V_0}{s} \cdot \frac{1}{Z_0 \left[ 1 + \frac{Z_L \cosh(\tau s) + Z_0 \sinh(\tau s)}{Z_0 \cosh(\tau s) + Z_L \sinh(\tau s)} \right]}$$

$$= \frac{V_0}{s Z_0} \cdot \frac{1}{\coth(\tau s) + 1} + \frac{V_0}{s(Z_0 + Z_L)} \cdot \frac{\cosh(\tau s) - \sinh(\tau s)}{\cosh(\tau s) + \sinh(\tau s)}$$

$$= \frac{V_0}{s Z_0} \cdot \frac{1}{\coth(\tau s) + 1} + \frac{V_0}{s(Z_0 + Z_L)} \cdot e^{-2\tau s}. \quad (\text{A.1})$$

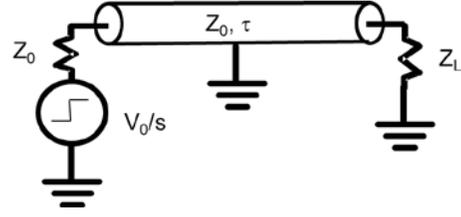


Figure A.1. Transmission line model of CCDM or CC-TLP.

The first term of the last expression is the TLP current into  $Z_0$  from an open circuited ( $Z_L = \infty$ ) line [12], [13] as in Fig. A.1, i.e., a calibration pulse. The second term is the current through  $Z_L$ , which will at least include the device current, and the exponential is the expected round-trip transmission line delay of  $2\tau$ . The second term of (A.1), exclusive of delay, is the device current. This is true both for CC-TLP (Figure 3) in which the applied pulse *charges* the device, as well as CDM2 (Figure 4) in which the applied pulse *discharges* the device. For charge-down,  $Z_L = \infty$  at  $s=0$  is required, as with series capacitance.

For low impedance CCDM (Figures 5-6),  $Z_L$  should be decomposed into two parts as in Fig. A.2: the removable device  $Z_d(s)$ , and the fixed  $Z_p$ , which includes a shunt resistor, if any, plus the exit transmission line (usually another  $Z_0$ ), in parallel with the shunt resistor. The resistor and matched exit line preclude the charge-down mode, but enable a “through” pulse for measurement. Let this measured pulse be  $V_p$ ,  $I_p$ , where  $V_p/I_p = Z_p$  whether  $Z_d(s)$  is connected or not. Let the near-end (reflected) measured current be  $I_m$ . Eq. (A.1) leads us to

$$I_m(s) = \frac{V_0}{s} \cdot \frac{Z_p + Z_d(s)}{(Z_0 + Z_p)(Z_{p0} + Z_d(s))}, \quad (\text{A.2})$$

where 
$$Z_{p0} = \frac{Z_p Z_0}{Z_p + Z_0}. \quad (\text{A.3})$$

Similarly, transmitted current into  $Z_p$  is

$$I_p(s) = \frac{V_0}{s} \cdot \frac{Z_d(s)}{(Z_0 + Z_p)(Z_{p0} + Z_d(s))}. \quad (\text{A.4})$$

But also from current division, device current

$$I_d(s) = \frac{V_0}{s} \cdot \frac{Z_p}{(Z_0 + Z_p)(Z_{p0} + Z_d(s))} = I_m(s) - I_p(s). \quad (\text{A.5})$$

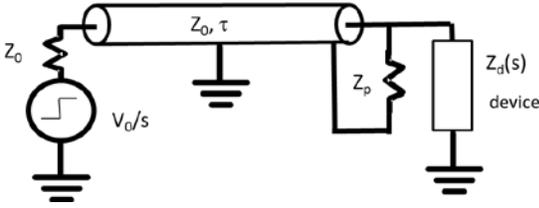


Figure A.2. Low-Z CCDM model;  $Z_p$  represents through line and shunt resistor.

Thus we have a way to measure device current with reflected and transmitted signals with the device in place. But what if we want to avoid setting up the reflection measurement  $I_m$ ? Again,  $V_p/I_p=Z_p$ , but now  $V_p$  is  $V_{\text{transmitted}}$  from Sections II.B and II.C when  $Z_d$  is connected. Meanwhile,  $V_{\text{rfr}}$  from Section II.C is  $V_p$  with no device, or

$$V_{\text{rfr}}(s) = \frac{V_0}{s} \cdot \frac{Z_p}{(Z_0 + Z_p)} = \frac{2Z_p}{(Z_0 + Z_p)} V_i = 2Z_{p0} I_i. \quad (\text{A.6})$$

The coefficient of  $V_i$  is the transmission coefficient and identical to  $(1+\Gamma)$  in Eq. (7).  $I_i=V_i/Z_0$ . But  $I_m=I_i-I_r$ , thus  $I_d=I_i-I_r-I_p$  ( $I_r$  being reflected current, and  $I_r = V_r/Z_0$ ). However  $V_{\text{rfr}}=I_{\text{rfr}}Z_p=V_r+V_i$  also. Eliminating  $I_i$  and  $I_r$  from these equations gives

$$I_d = (I_{\text{rfr}} - I_p) \left(1 + \frac{Z_p}{Z_0}\right) = \frac{V_{\text{rfr}} - V_{\text{transmitted}}}{Z_{p0}}. \quad (\text{A.7})$$

This agrees with Eq. (8) in II.C. It can also be shown that

$$I_d = (I_m - I_{\text{rfr}}) \left(1 + \frac{Z_p}{Z_0}\right), \quad (\text{A.8})$$

thereby allowing all-reflection measurements. Thus from (A.5), (A.7), and (A.8), any two of the quantities  $I_m$ ,  $I_p$  and  $I_{\text{rfr}}$  are sufficient for determining  $I_d$ , while all three allow redundant self-checking of the setup. If  $Z_p$  is a shunt resistor  $R_x$  in parallel with exit line of impedance  $Z_t$ , then  $Z_p=R_x Z_t/(R_x+Z_t)$ , but usually  $Z_t=Z_0$ .

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